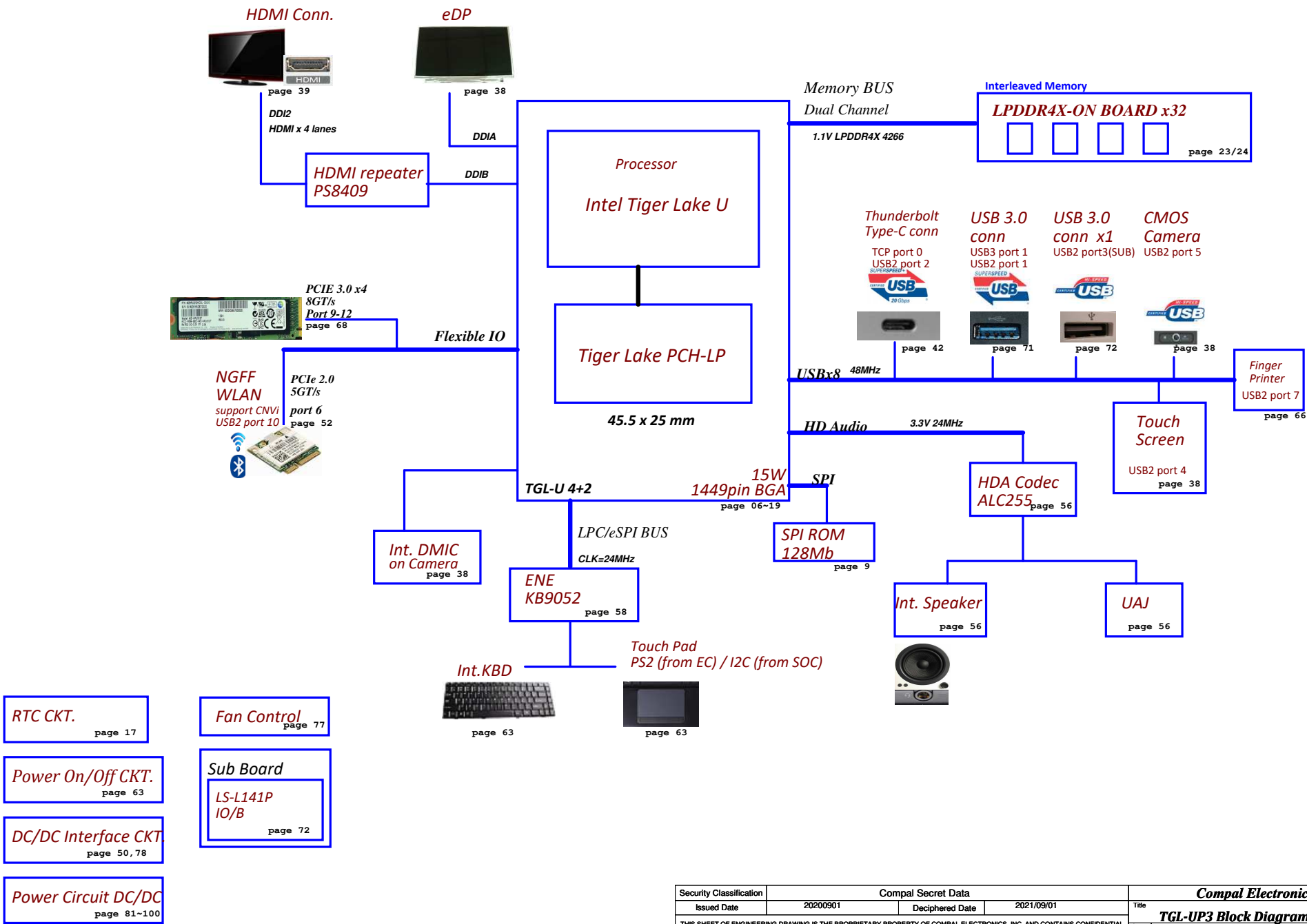


Compal LA-L151P
GH4UT MB Schematic Document
Rev: 1A
2021.01.14-B

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					LA-L151P
				Date:	Thursday, January 14, 2021
				Sheet	1 of 102
				Rev	1A



Vcc	3.3V +/- 5%	EC Board ID Table for AD channel				*PCB Version
Ra	100K +/- 1%					*Key board type
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0	0		0.000 V	0.300 V	0x00 - 0x13	SD028000080
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	SD034120280
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	SD034150280
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	SD034200280
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	SD034270280
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	SD034330280
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	SD034430280
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	SD034560280
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76	SD034750280
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87	SD034100380
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96	SD034130380
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4	SD034160380
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF	SD034200380
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7	SD000001B80
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	SD00000G280
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9	SD034330380
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4	SD00000WM80
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD	SD034560380
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0	SD00000AL80
19	NC	3.000 V	3.000 V		0xF1 - 0xFF	NC

Board ID	PCB Revision
0	PCB Rev 0.1
1	PCB Rev 0.2
2	PCB Rev 1.0
3	PCB Rev 1A
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

EVT@
EVT2@
PVT@
MP@

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
SOC_CK/DA (Port0)				
SOC_CK/DA (Port3)	TM-P3393-003 (Touch Pad)			
SOC_SMBCLK	DIMM1			
EC_CK/DA (Port0) (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_CK/DA (Port1) (+3VS)	TGL-U / PCH LP	TBD		
SOC_SML1CK/DA (+3VALW)	Thermal Sensor (NCT7718W)	0x98	1001_1001b	1001_1000b
	Thermal Sensor (G781)	0x9A	1001_1011b	1001_1010b
	Thermal Sensor (G753)	0x90		
EC_CK/DA (Port2)				
EC_CK/DA (Port3)	TI PD	0x40		
EC_CK/DA (Port4)	N/A (Set GPIO)			
EC_CK/DA (Port5)				

Re-Timer 0x55 TBC 0x30

PCB@_ZZZ9
PCB
DAB0008F000

V : Must V : Options

Item (X43 / X76)	BOM Structure	Item (X43 / X76)	BOM Structure
Unpop	@	POWER	3S@ V
Connector	CONN@	Thermal	TMS@ V
R Short	short@	Finger print	FP@ V
Debug conn.	DEBUG@	TPM	TPM@
PCB	PCB@ V	Touch screen	TS@
CMC	CMC@ V	Touch screen-US8	US8TS@
EC BID	PVT@ V	Touch screen-I2C	I2CTS@
SOC	MP@ V	AUDIO	255@ V
SOC	PREM@ V	AUDIO	255M@
SOC	VOL@	AUDIO	256@
SOC	CLITCH@ V		
SOC	NRTD3@ V	USB Off-line chg	NCHG@
SOC	RTD3@	USB Off-line chg	CHG@ V
SOC	VPRO@		
SOC	SPK02@	CNVI	CNVI@ V
SOC	SPK05@	Type-C	TypeC@ V
SOC	SPK08@		
Memory Down	MEMDIE@		
Without MD	NODX76@		
HYNIX	X76HYN16G@		
	X76HYN8G@		
SAMSUNG	X76SAM16G@		
	X76SAM8G@		
MICRON	X76MIC16G@		
	X76MIC8G@		

Item (X4E)	BOM Structure
EMI requirement	EMI@ V
EMI require reserve	XEMI@ @EMI@
ESD requirement	ESD@ V
ESD require reserve	XESD@ @ESD@
RF requirement	RF@ V
RF require reserve	XRF@ @RF@
FP EMI requirement	FP EMC@ V
FP ESD requirement	FPESD@ V
X4E	FOR MB EE
X4E	FOR IO EE

EMC@ V
XEMC@
@EMC@
BL_EMC@ V
BL_EMI@ V
BL_ESD@ V

STATE	SIGNAL	SLP_S0P	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
SOIX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Power Plane	Description	S0	S0ix	S3	S4/S5
+19V_ADPIN_P1	Adapter power supply	N/A	N/A	N/A	N/A
+20V_PDVIN	PD USB-C power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery power supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6V_VDDQ	LPDDR4x +0.6V power rail(VDDQ)	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.1V_VDDQ	LPDDR4x +1.1V power rail (VDD2)	ON	ON	ON	OFF
+1.8V	LPDDR4x +1.8V power rail(VDD1)	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	ON	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DS	+3VALW power for PCH DS	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

BOM Number	Load BOM Option
431AQFBOL01	SRK08@/PCB@/X76MIC8G@/255@/3S@/CHG@/CMC@/CNVI@/EVT@/FP@/GLITCH@/MP@/TMS@/TypeC@/PREM@/NRTD3@/TPM@

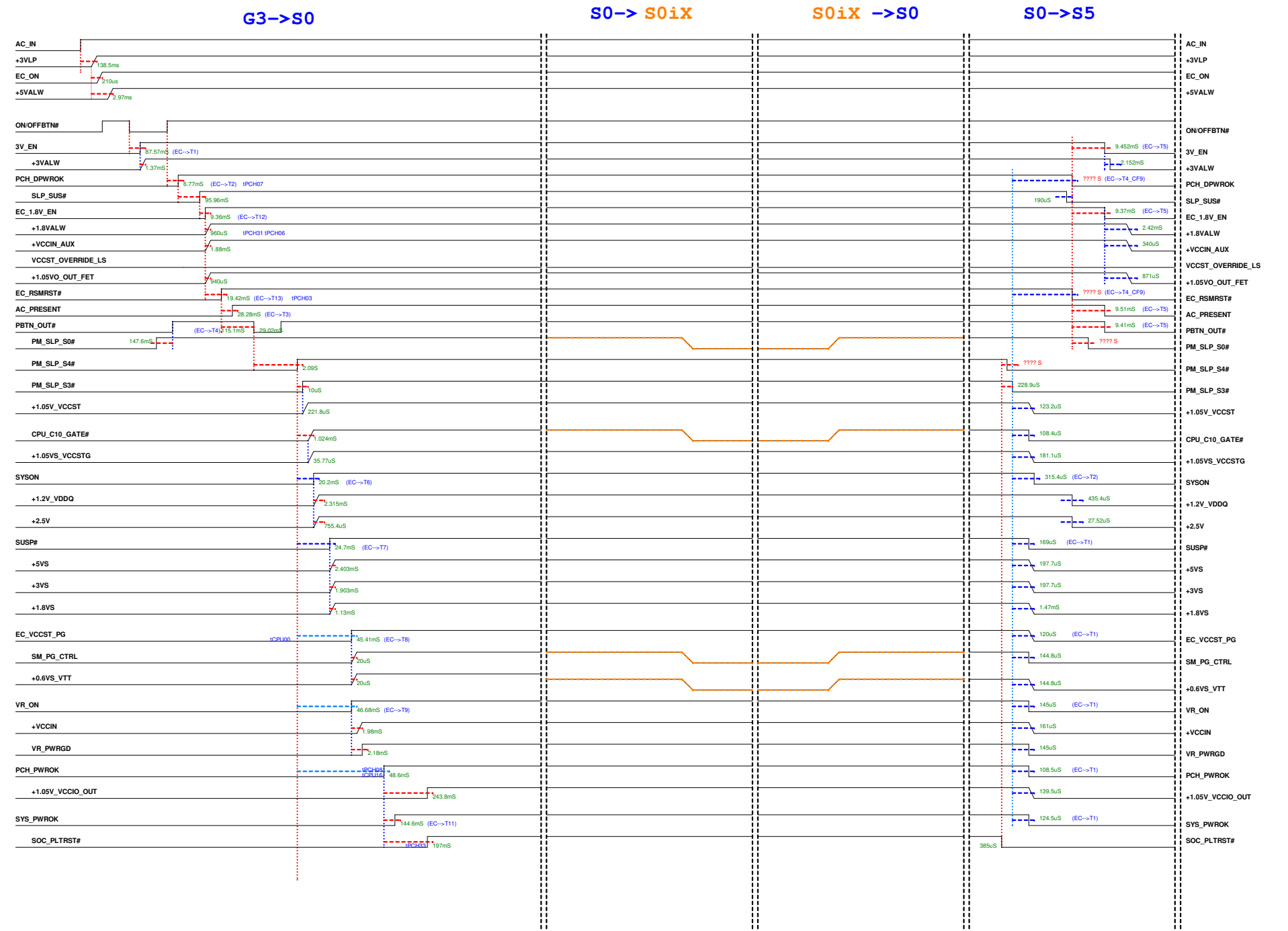
Load BOM Option Table for Baseline

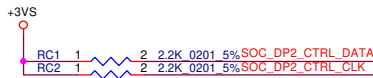
BOM Number	Load BOM Option
X4EAQFBOL01	EMI@/ESD@/FP EMC@/FPESD@/BL_EMC@/BL_ESD@/EMC@/BL_EMI@/RF@



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				LA-L151P	Rev 1A
Date:		Thursday, January 14, 2021		Sheet	4 of 102

[GH4UT - AC PWR Sequence_TGL-UP3_LPDDR4X_S0iX]

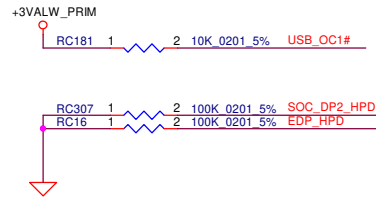
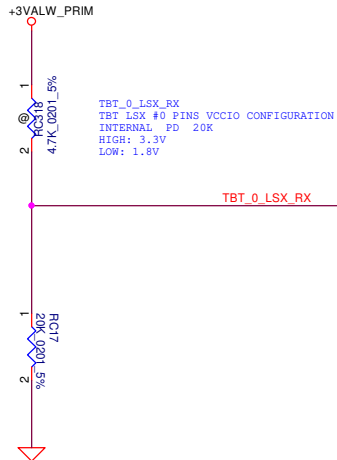
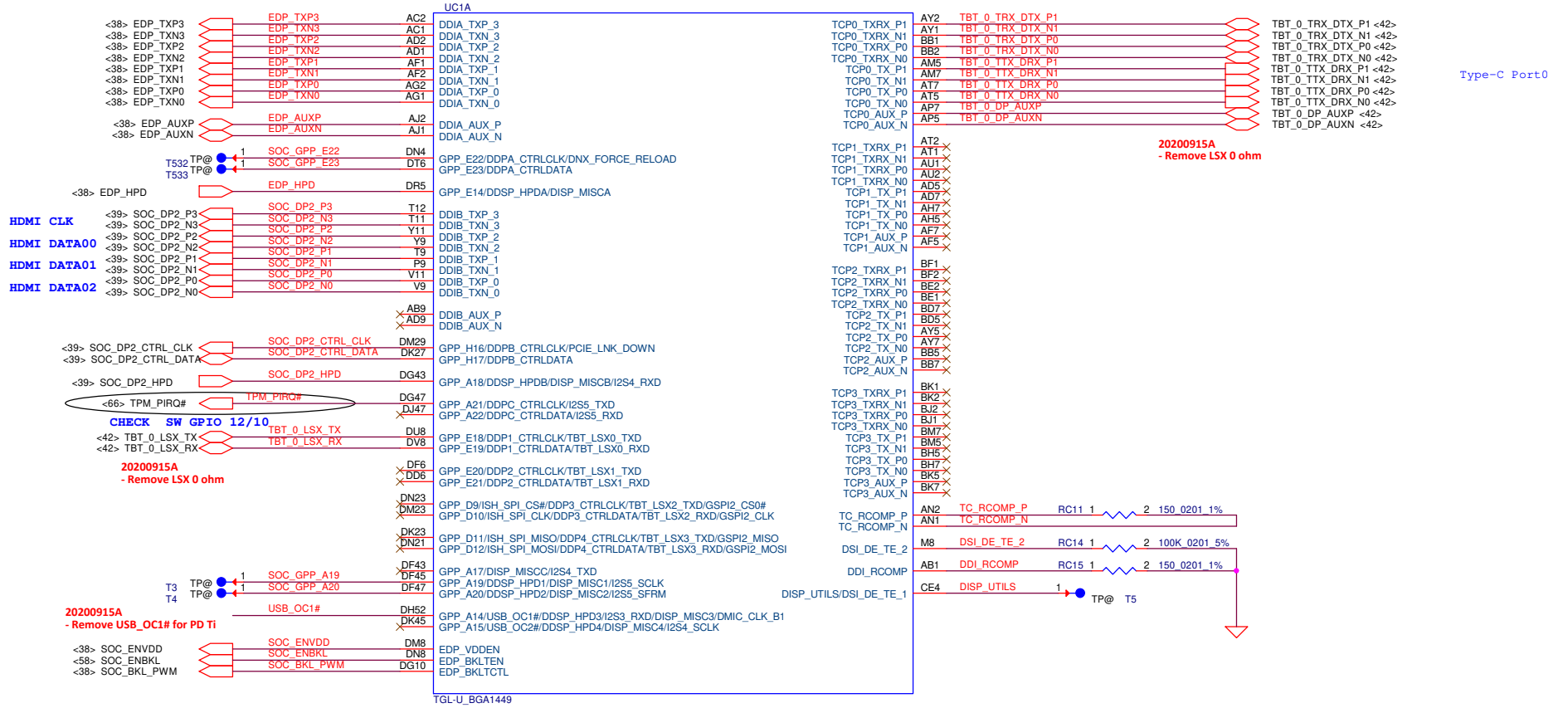




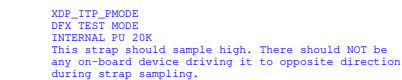
UC1

S IC FH8069004530104 SRK02 B1 2.8G ABO 1

SA0000DTT30



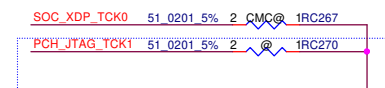
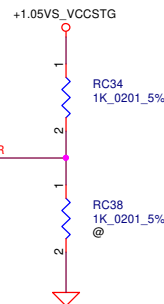
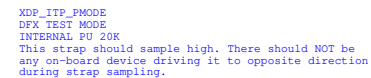
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				Date: Thursday, January 14, 2021			Sheet	6	of 102



PVT: add for M2 SSD RTD3



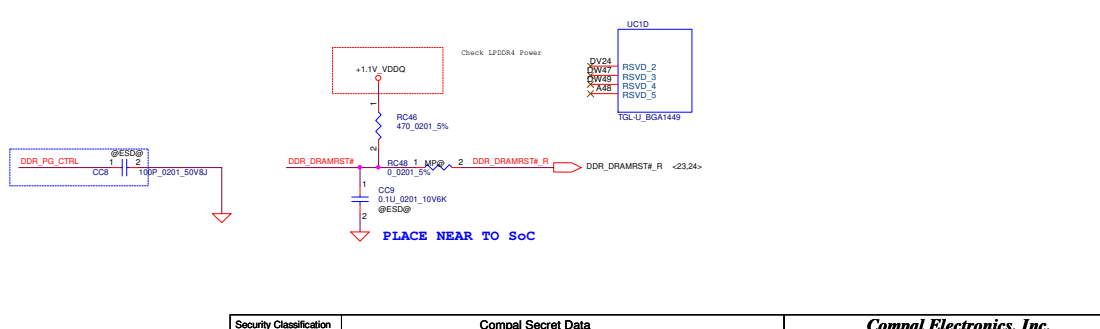
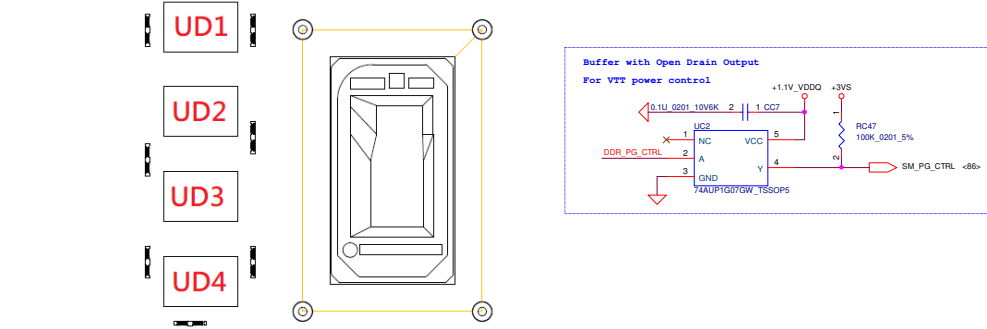
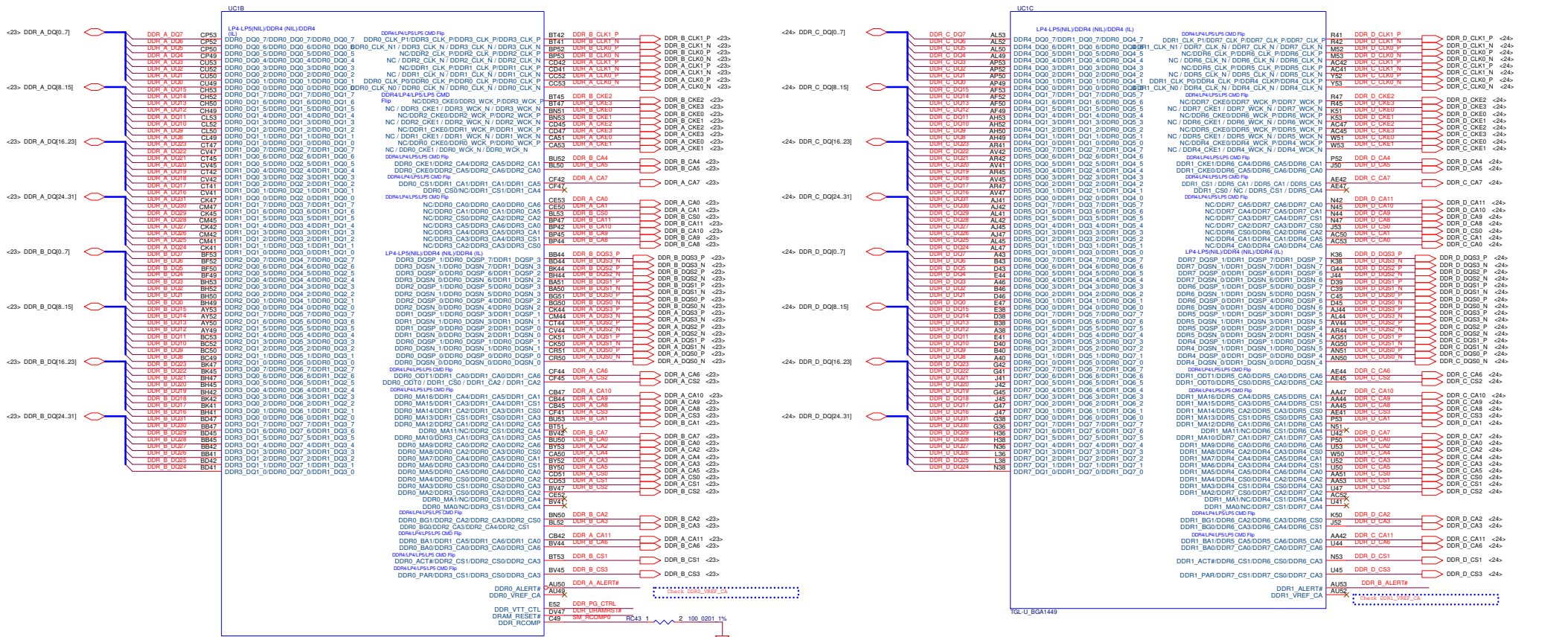
SOC_WWAN_RST#
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
INTERNAL PD 20K



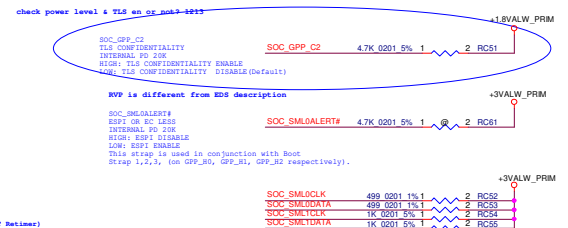
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				LA-L151P		
				Date:	Thursday, January 14, 2021	Sheet 7 of 102

Follow Intel LPDDR4 NII

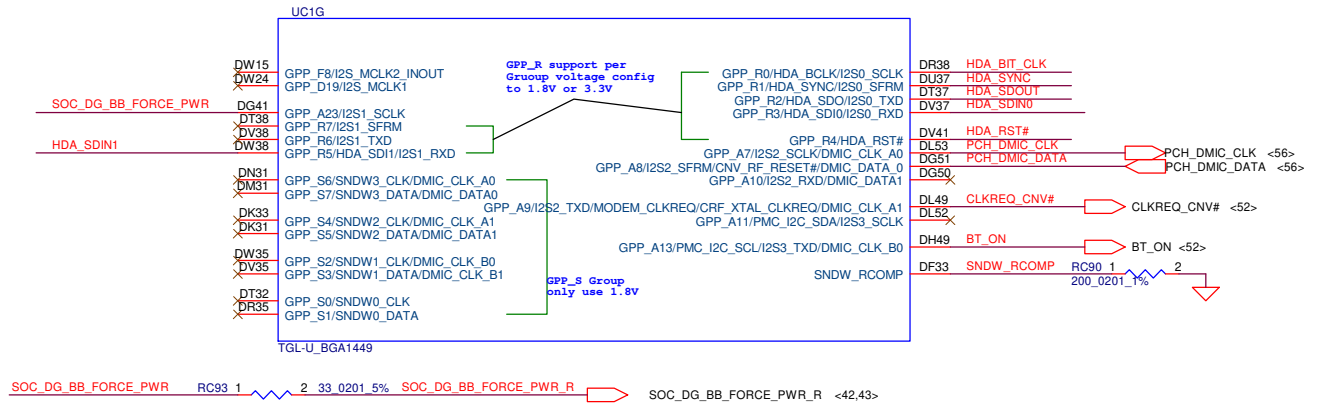
LPDDR4: Refer to 612304_TGL_LPDDR4_RVP_SCH_REV0P7



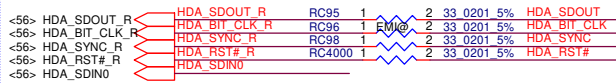
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LA-151P			
Thursday, January 14, 2021			
Sheet 8 of 102			



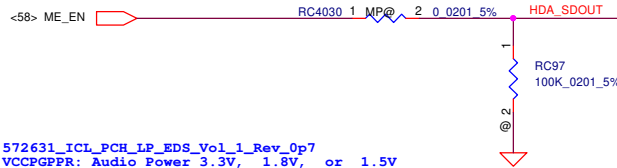
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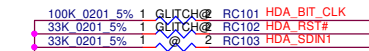
HDA for AUDIO



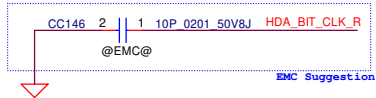
To Enable ME Override



572631 ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

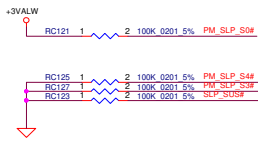


Follow
607872_TGL_UY_PDG for Glitch



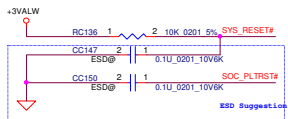
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Issued Date				20200901		Deciphered Date		2021/09/01		Title	
										TGL-UP3(5/14)HDA,SNDW	
										Rev 1A	
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										Sheet 10 of 102	

Follow
607872_TGL_UY_PDG_Rev0p5 for Glitch

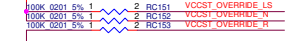
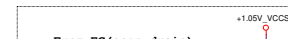
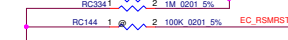
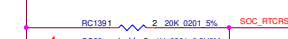
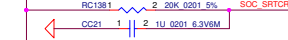


WLAN

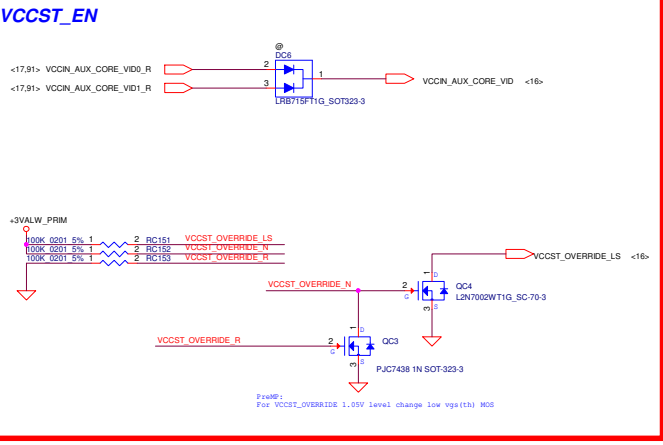
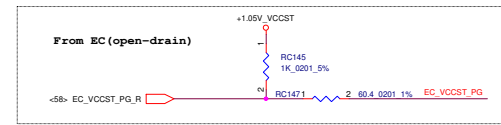
SSD GEN3
SSD GEN4
20201016A
- ADD SSD GEN4



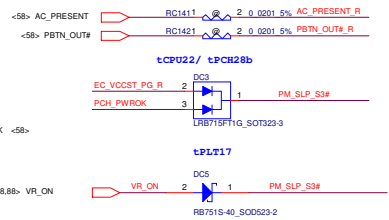
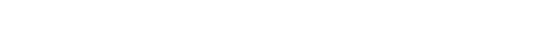
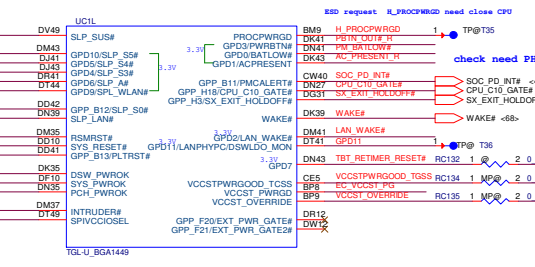
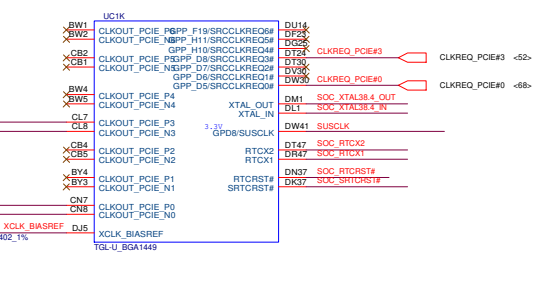
ESD Suggestion



PSG 4.2.5
INTRUDER# should have a weak external pull-up to VccRST

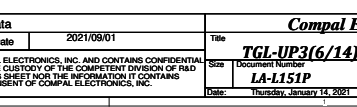
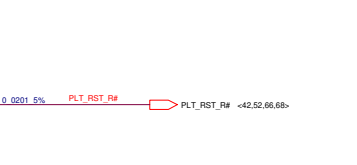
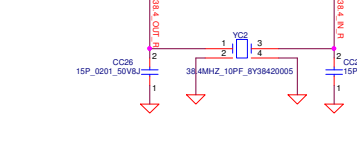
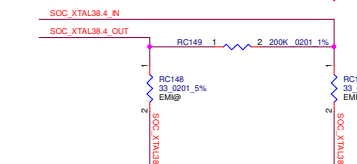
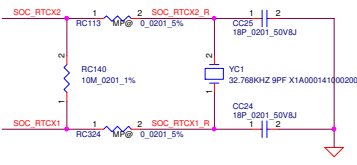
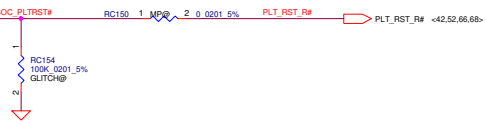


For VCCST_OVERRIDE 1.05V level change low vga(th) MOS

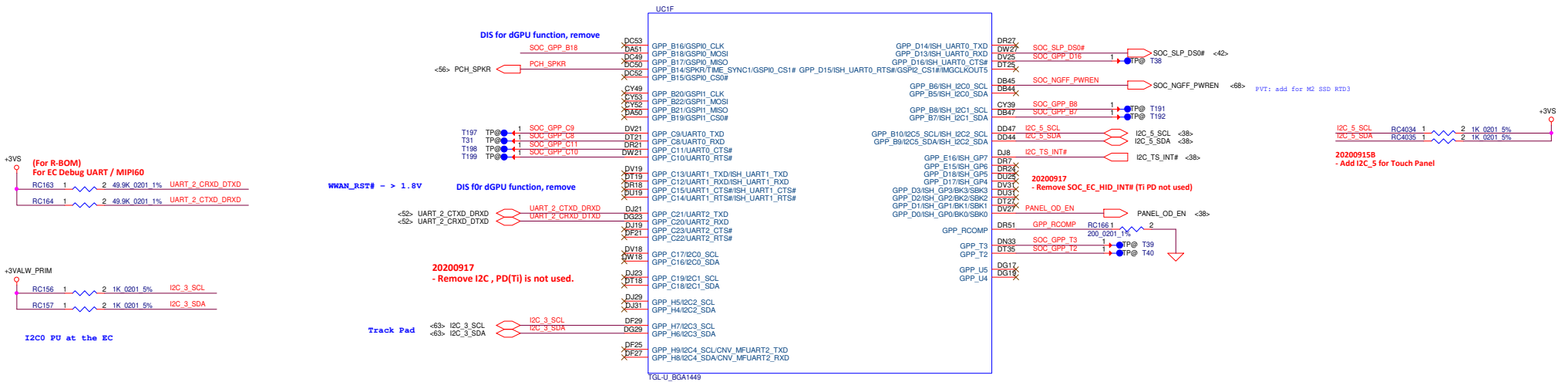


<58> VR_ON

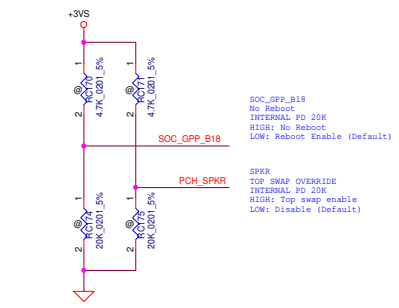
PCH PLTRST Buffer



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Date: Thursday, January 14, 2021				Sheet	11 of 102



Strap Pin



PDG 6.8.6
For integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVi) solution,
Tiger Lake PCH-LP USB 2.0 port # 10 must be used.

SSD (Gen3)

20201016A
- SSD Change to GEN4

WLAN (Gen2)

USB3.1 Type-A (SUB JUSB1)

20200914B
- Add for USB3 SUB

USB3.1 Type-A (MB JUSB1)

6.4.1 Flexible I/O Implementation
PCH-LP (UP3)

Figure 70. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
	USB 3.2 Gen 1x1/Zx1 #1	USB 3.2 Gen 1x1/Zx1 #2	USB 3.2 Gen 1x1/Zx1 #3	USB 3.2 Gen 1x1/Zx1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
HSIO Type and Lane	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4								

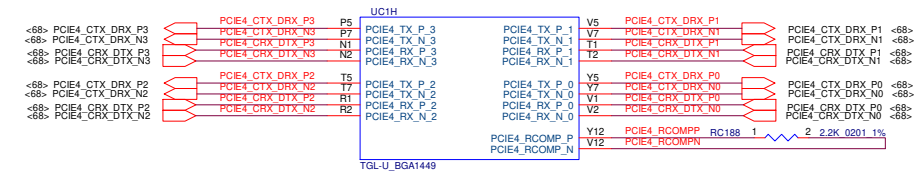
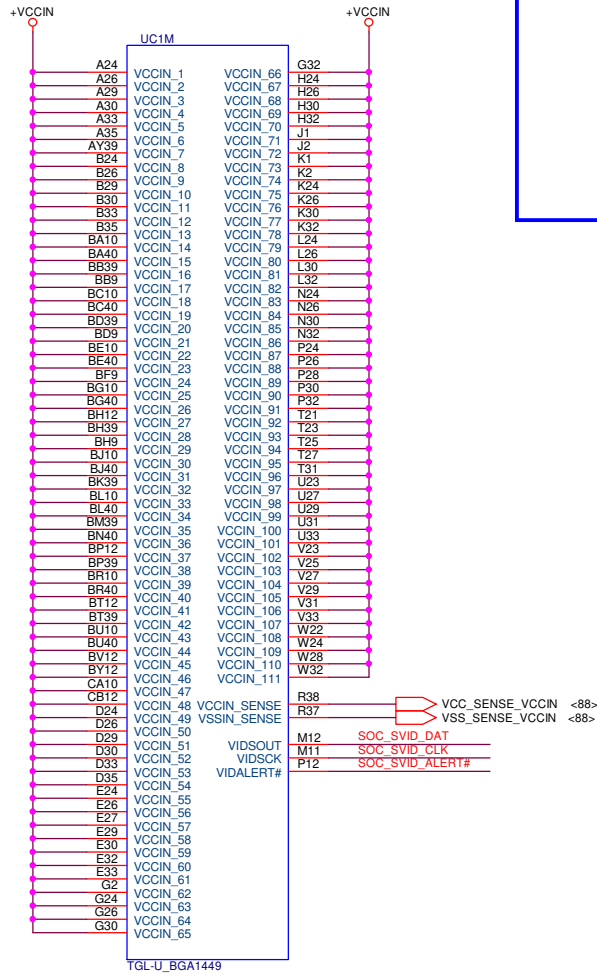


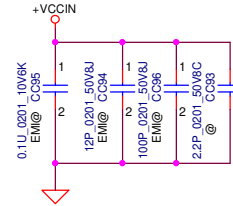
Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): • CLKOUT_PCIE_P[6:0] • CLKOUT_PCIE_N[6:0] PCH-LP (Y): • CLKOUT_PCIE_P[6:1] • CLKOUT_PCIE_N[6:1]	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

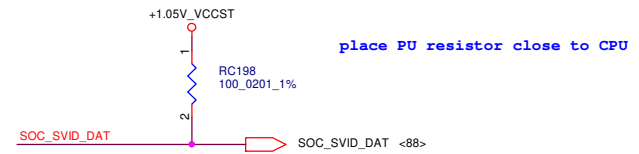


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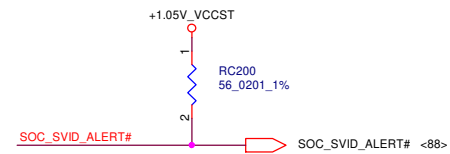
EMC CAPS-PLACE
< 5mm from SOC VCCIN



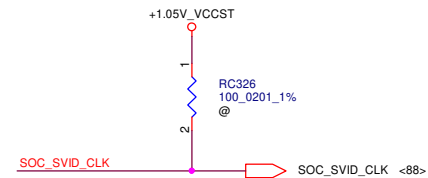
SVID DATA



SVID ALERT

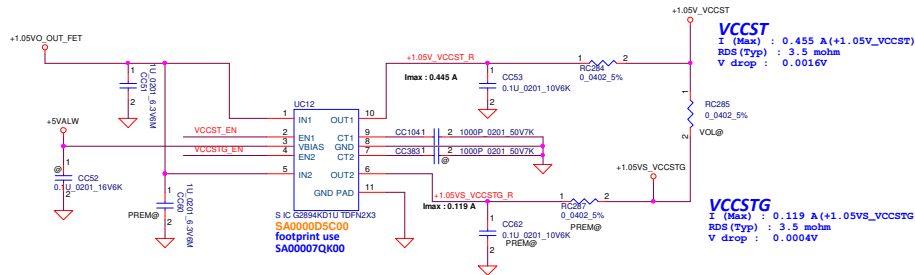
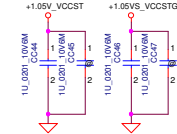
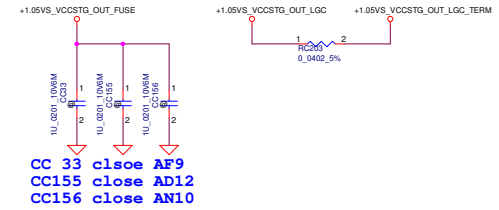
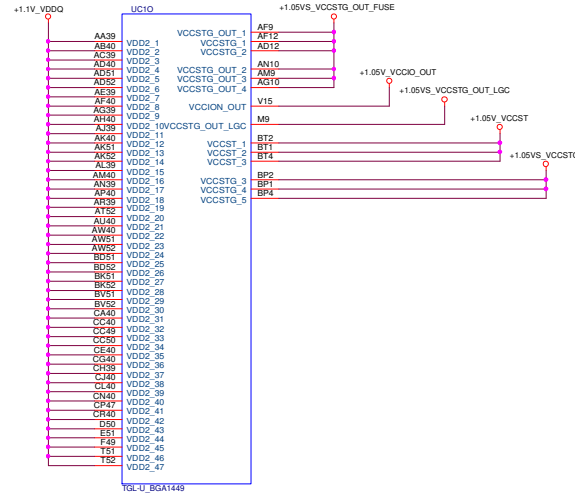
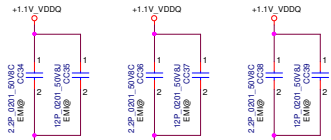


SVID CLOCK



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								LA-L151P		1A	
						Date:		Thursday, January 14, 2021		Sheet 15 of 102	

EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)



CC383 must be @
CPU_C10_GATE# stable to +1.05V_S VCCSTG <= 65us (tCPU26)

VCCST
I (Max) : 0.455 A (+1.05V_S VCCST)
RDS (Typ) : 3.5 mohm
V drop : 0.0016V

VCCSTG
I (Max) : 0.119 A (+1.05V_S VCCSTG)
RDS (Typ) : 3.5 mohm
V drop : 0.0004V

Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

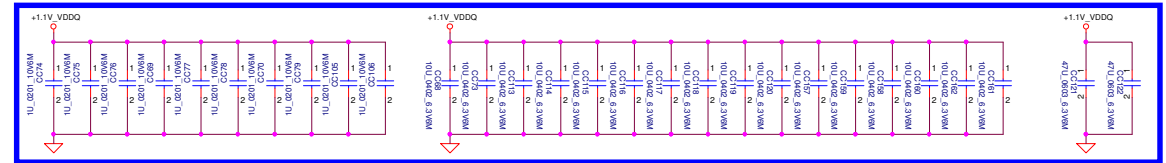


Figure 228. VCCST Enable Logic

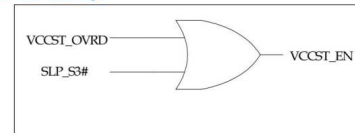
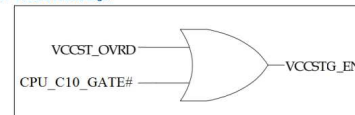
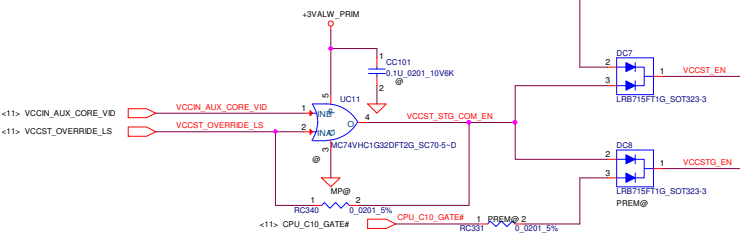


Figure 229. VCCSTG Enable Logic

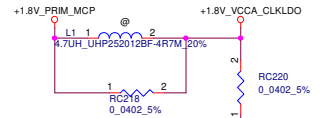
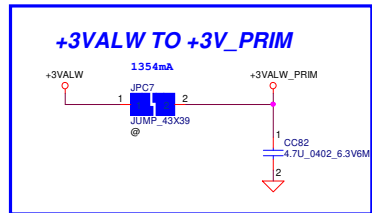
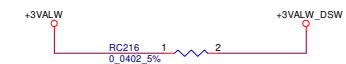
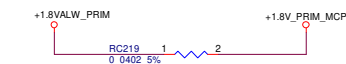


VCCST/VCCSTG Enable

ICL have EC_VCCST_EN
check need it? or use syson/susp? 1210

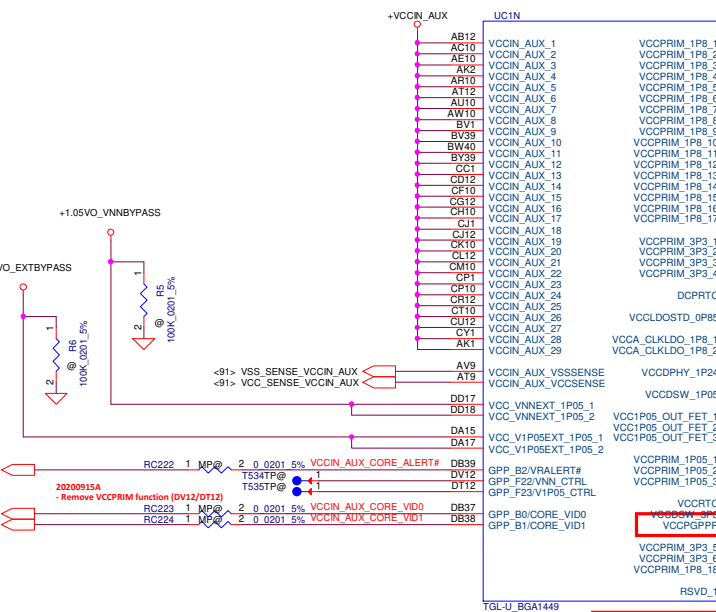
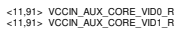
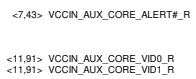
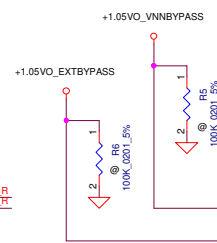
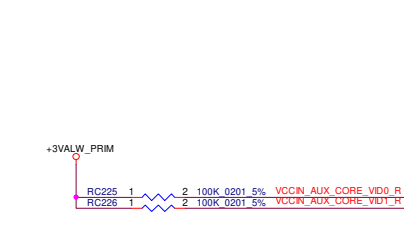
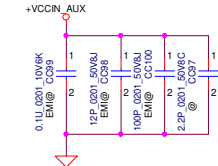


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				Date	Thursday, January 14, 2021
				Sheet	16 of 102

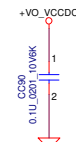
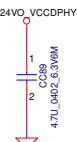
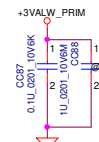
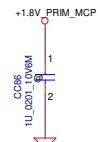
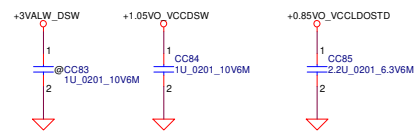
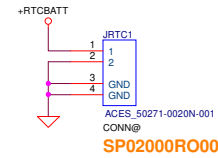
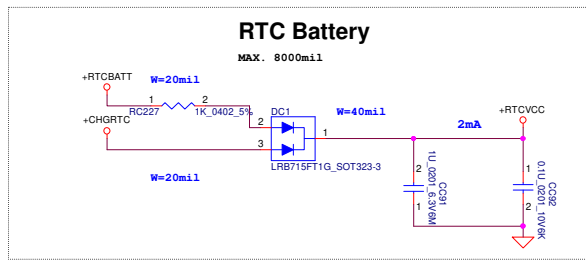


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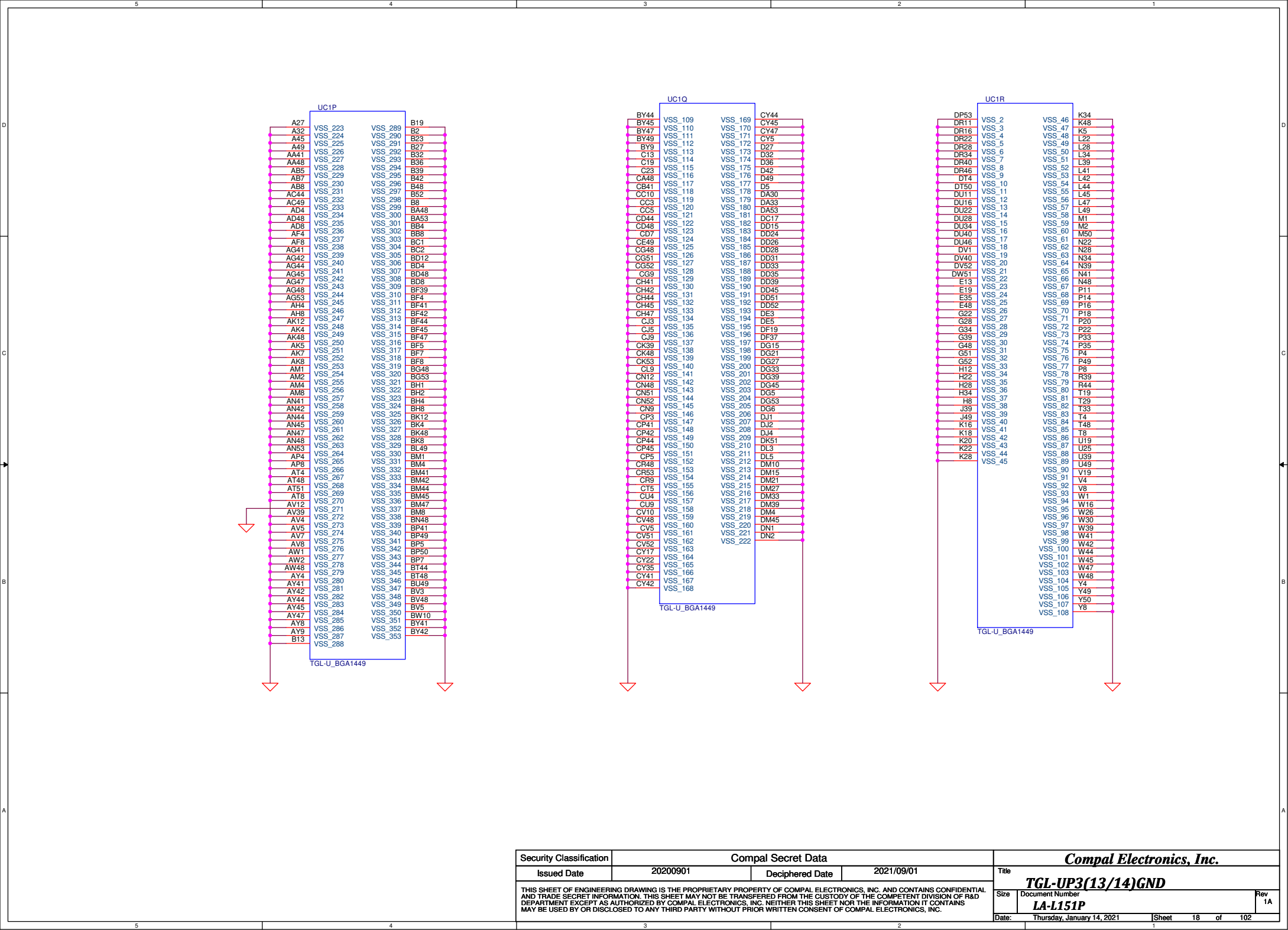
EMC CAPS-PLACE
< 5mm from SOC VCCIN_AUX



NOTE:
576591-tgl-pch-1p-ads-volof2-rev0p5
VCCGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.
607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCGPPR can be merged directly with
either VCCPRIM_1P8 or VCCPRIM_3P3 depending on their operating voltage.



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				Rev	1A
				Thursday, January 14, 2021	Sheet 17 of 102

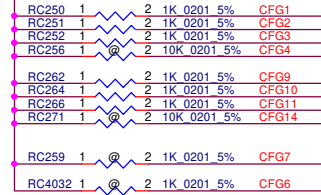


CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[5]	RSVD	None	1K ohm
CFG[6:7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	1K ohm
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: <ul style="list-style-type: none">- 1 - (Default) Normal- 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

20200915B
- Update Table (PDG 2.0)

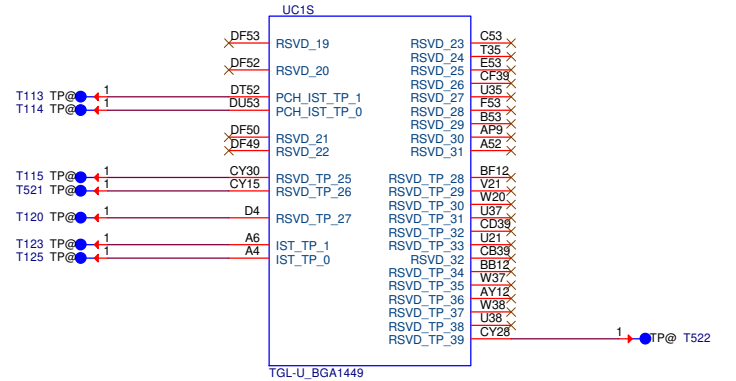
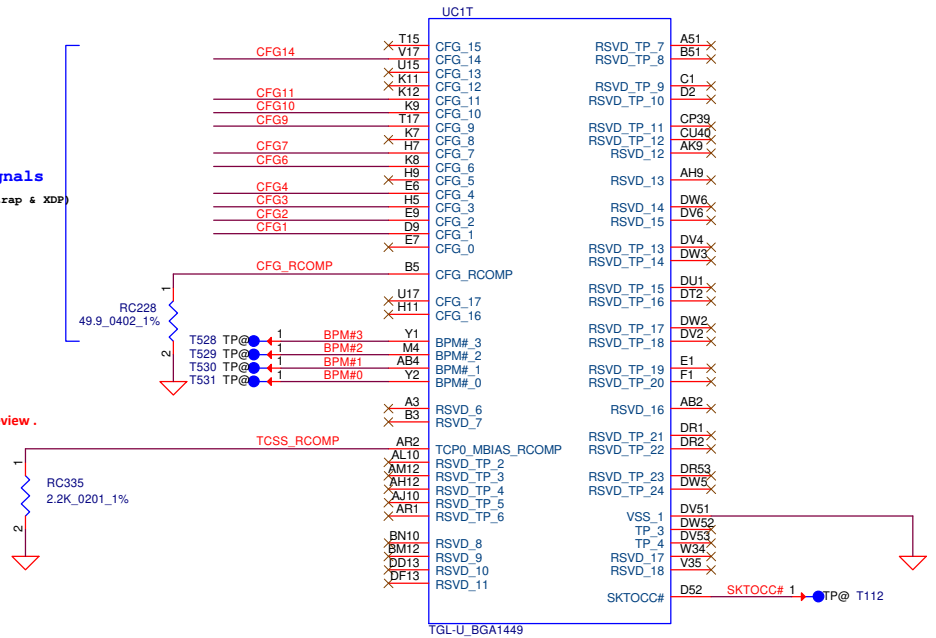
+1.05V_VCCIO_OUT



CFG14
PEG60 Lane Reversal
HIGH : (Default) Normal
LOW : Reversed

20200915B (Follow GH47H)
- RC259 change to 1k (CFG7) for PDG2.0 update .
- Add RC4032 1K PU & RC4033 1K PD (CFG6) for PDG2.0 update & Intel SCH review .

CFG Signals
(For Strap & XDP)



S IC FH8069004531602 SRK08 B1 3G ABO !
SRK08@
SA0000DTV50



S IC FH8069004531301 SRK05 B1 2.4G ABO !
SRK05@
SA0000DTU30



S IC FH8069004530104 SRK02 B1 2.8G ABO !
SRK02@
SA0000DTT30

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Size		Document Number						LA-L151P			
Date:		Thursday, January 14, 2021		Sheet		19		of 102			
								Rev 1A			



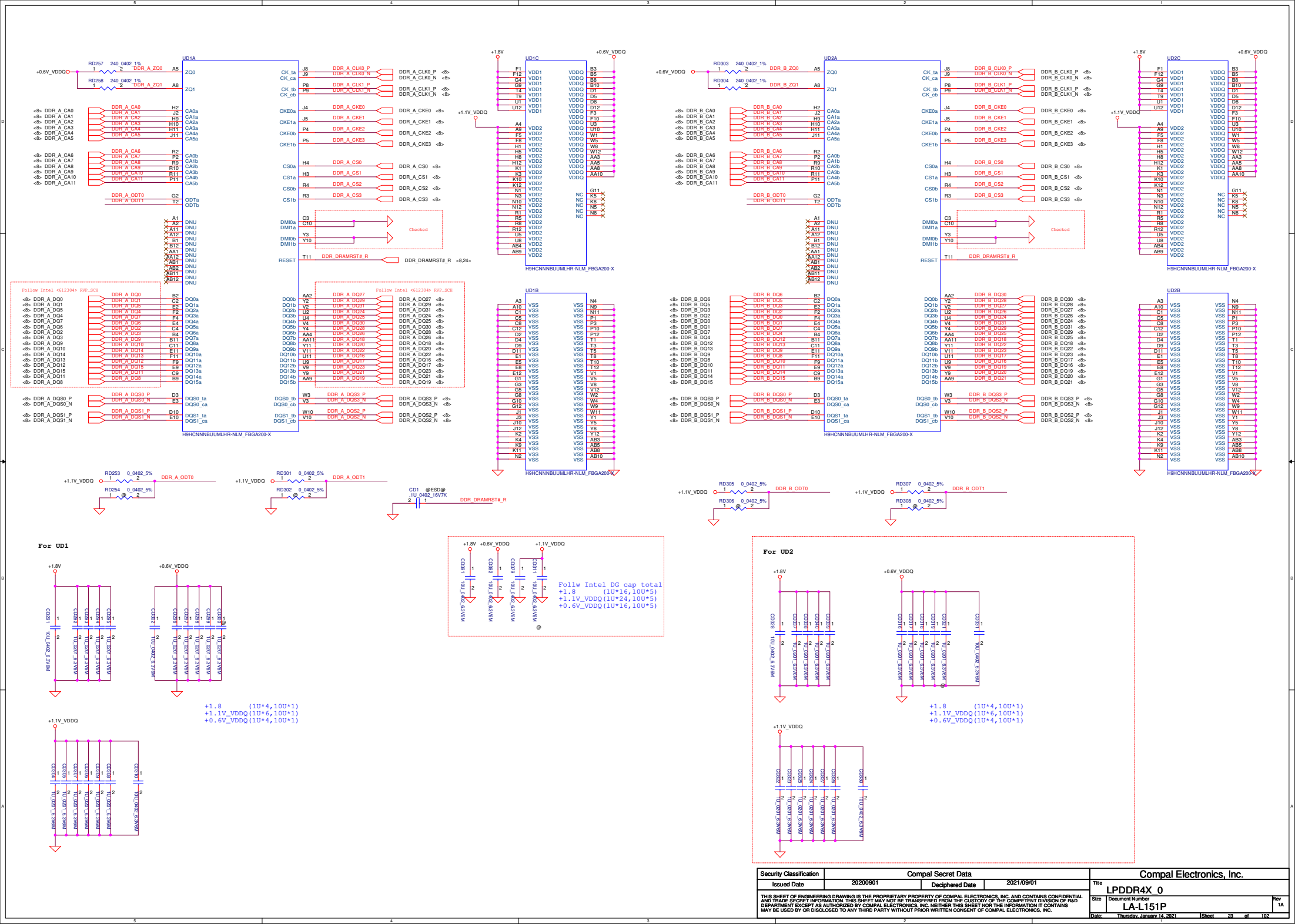
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								LA-L151P		1A	
						Date:		Thursday, January 14, 2021			
						Sheet		20 of 102			

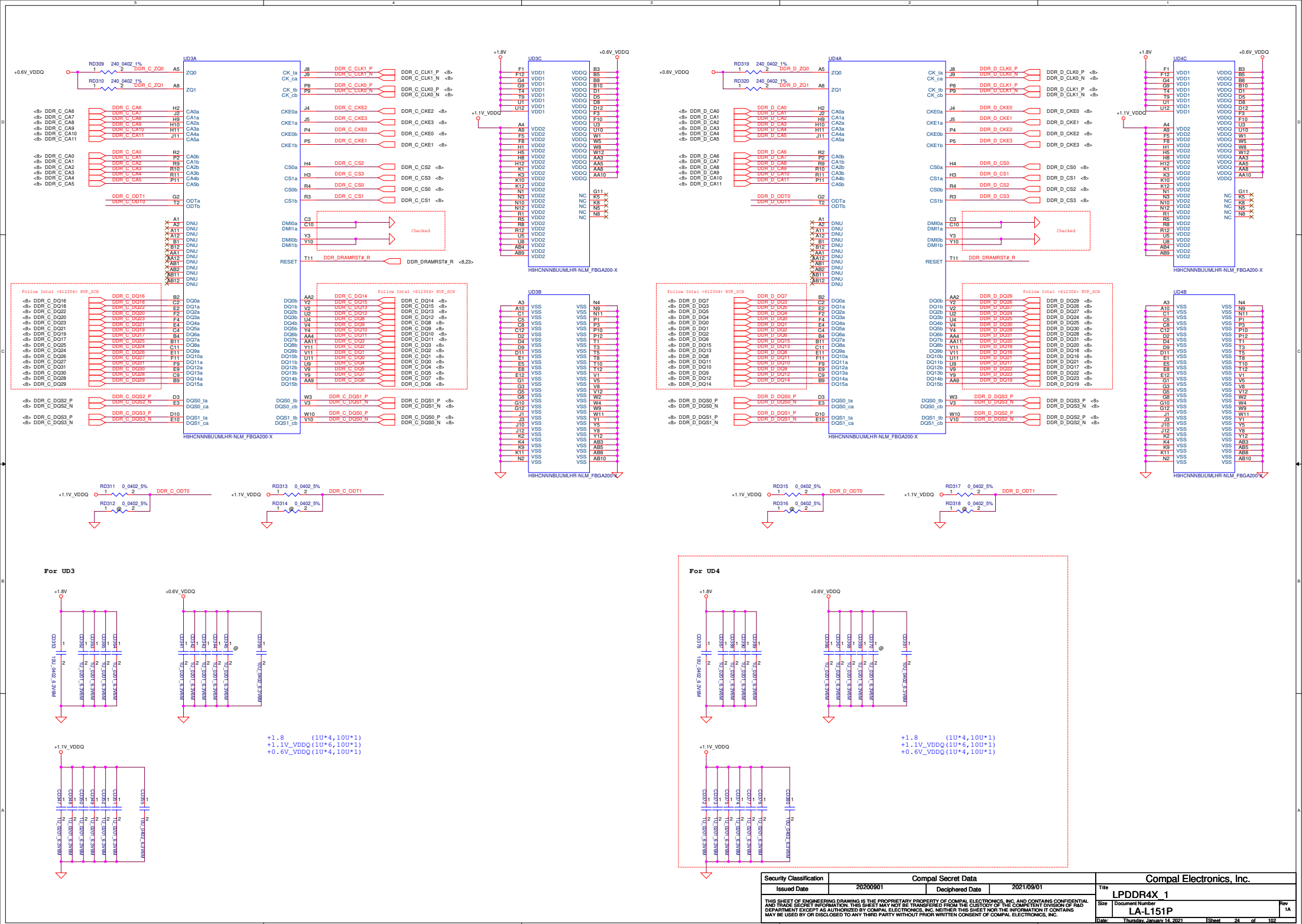


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							LA-L151P		1A			
						Date:	Thursday, January 14, 2021		Sheet	22	of	102



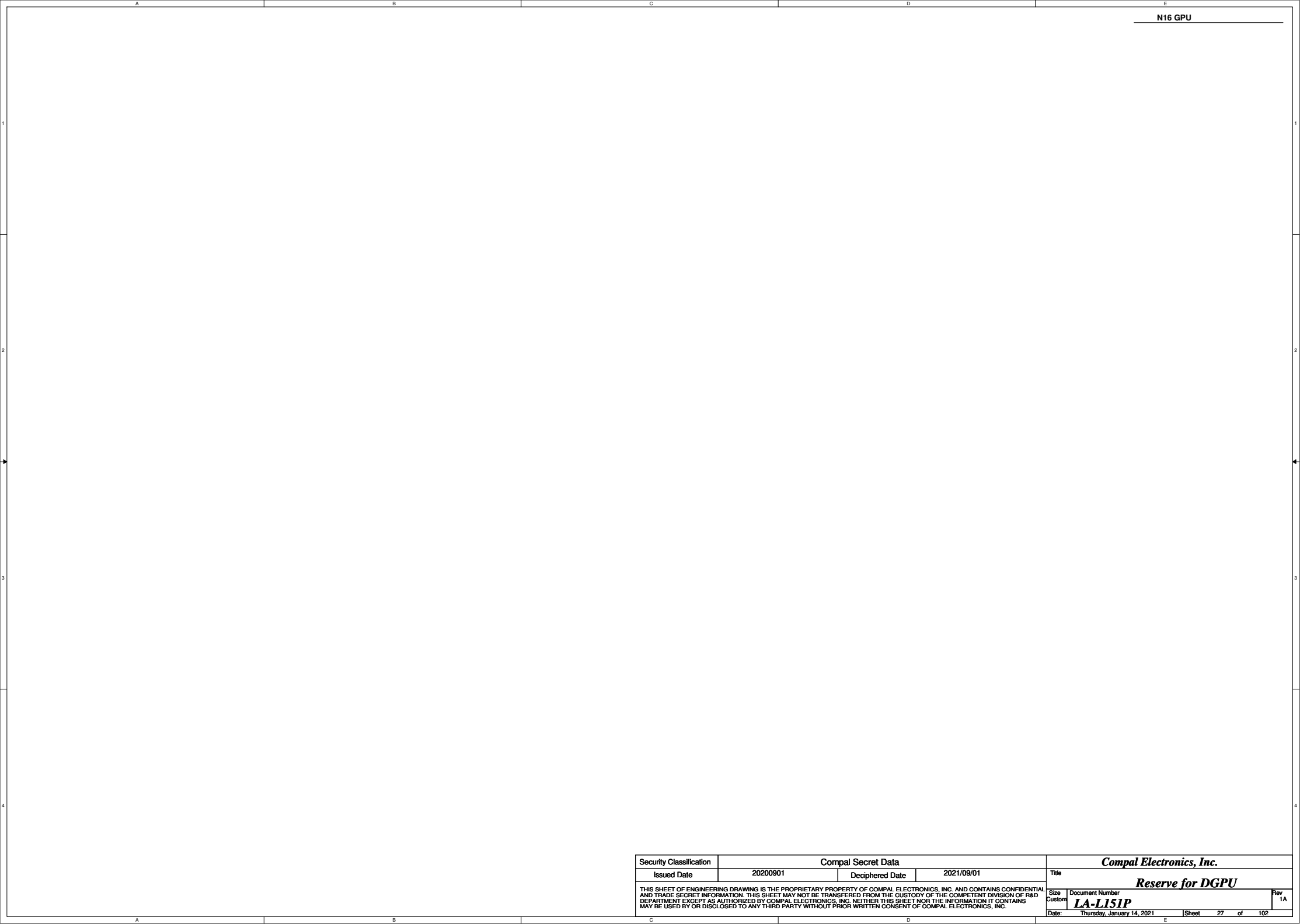




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						LA-L151P			1A		
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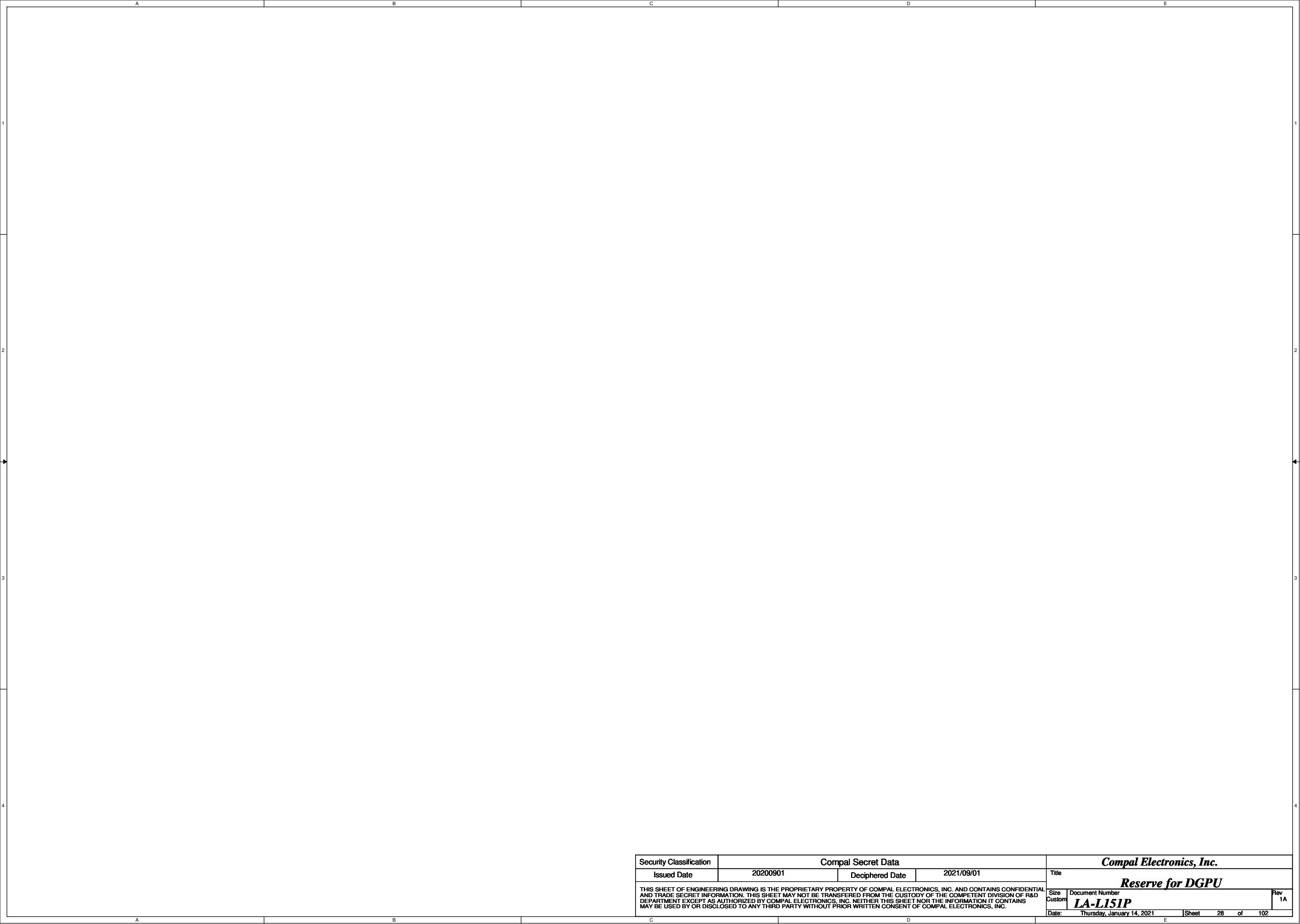


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									LA-L151P	1A	
Date:				Thursday, January 14, 2021		Sheet		26	of 102		

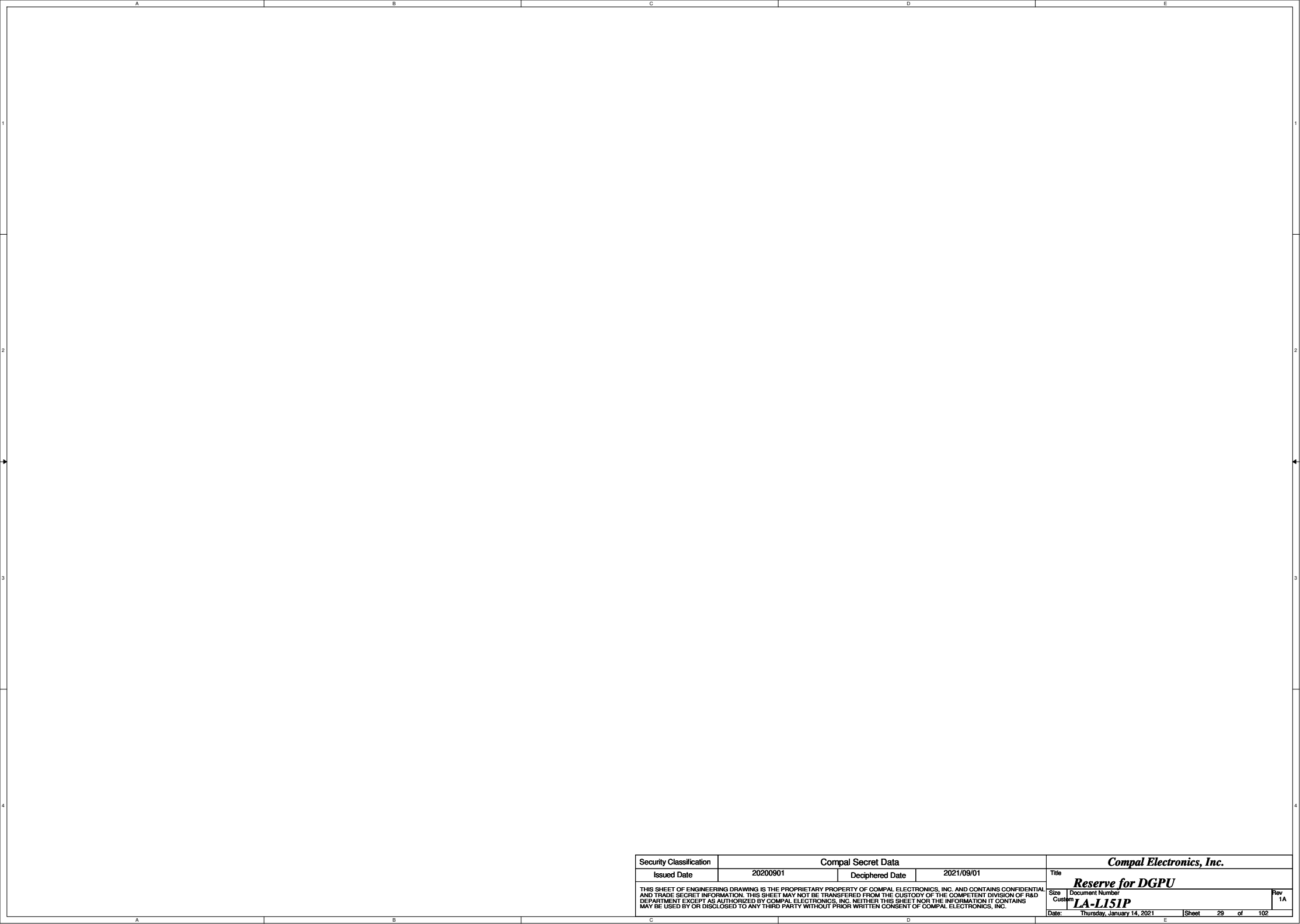


N16 GPU

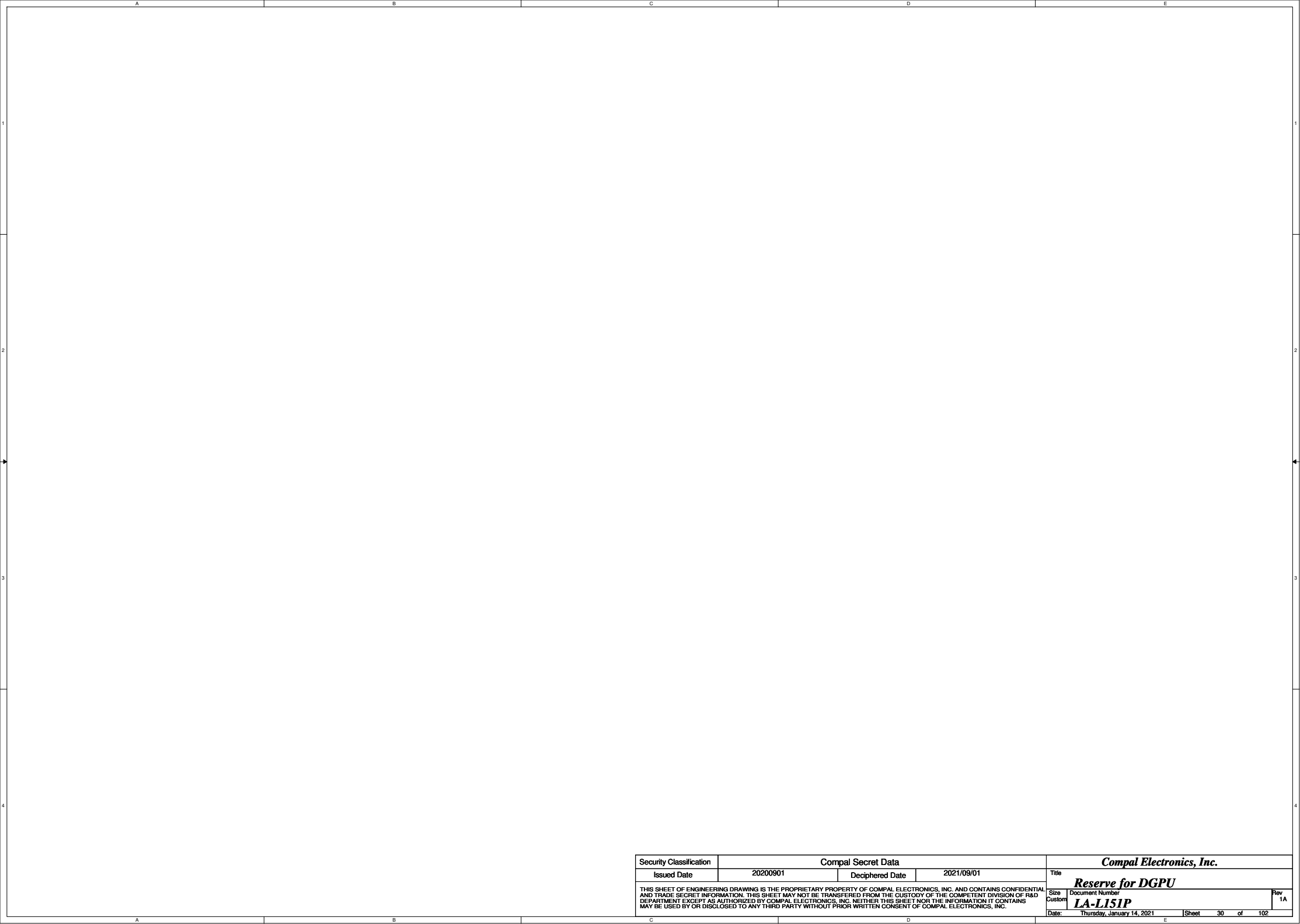
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				Date: Thursday, January 14, 2021	Sheet 27 of 102	



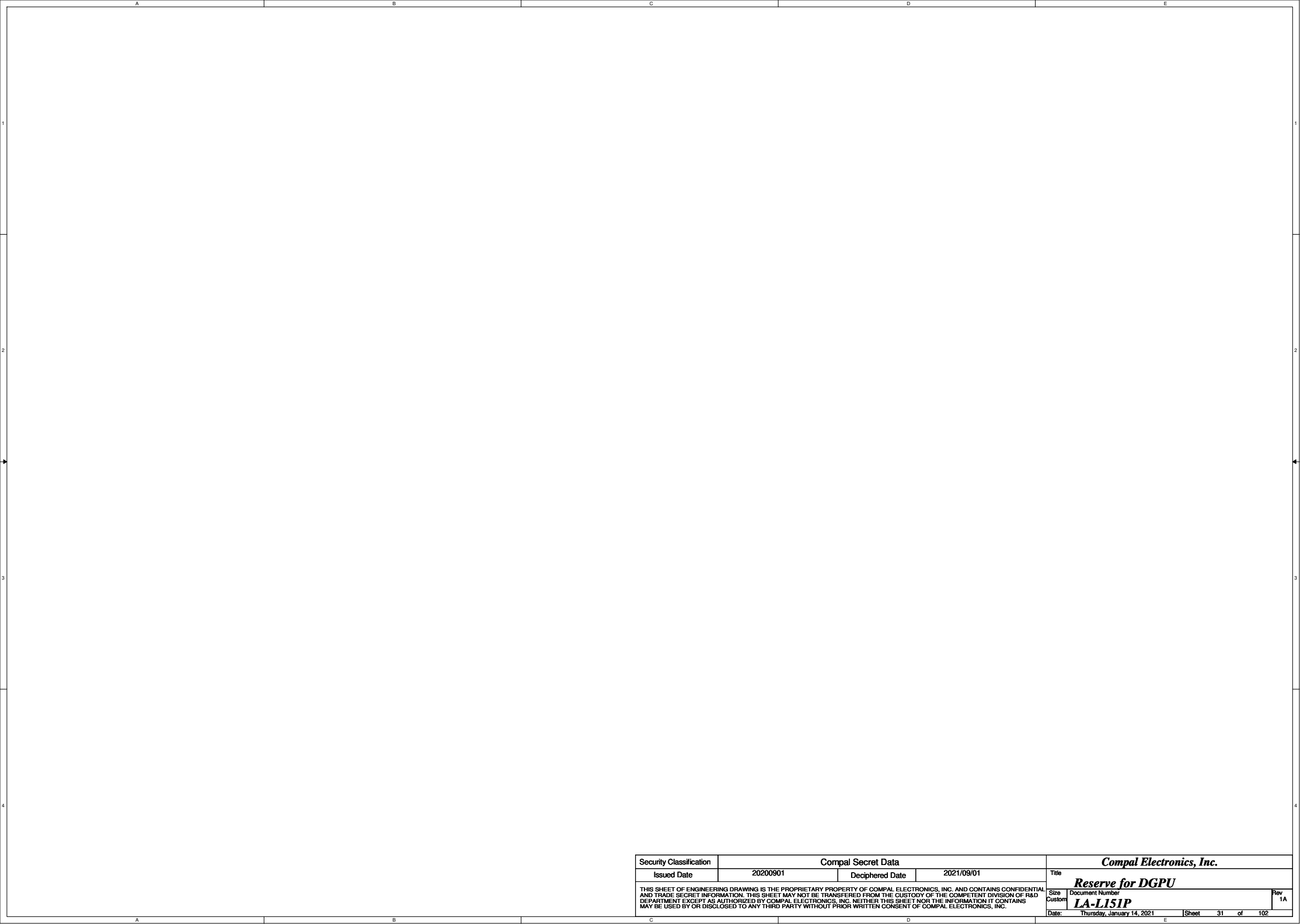
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				Thursday, January 14, 2021	Sheet 28 of 102



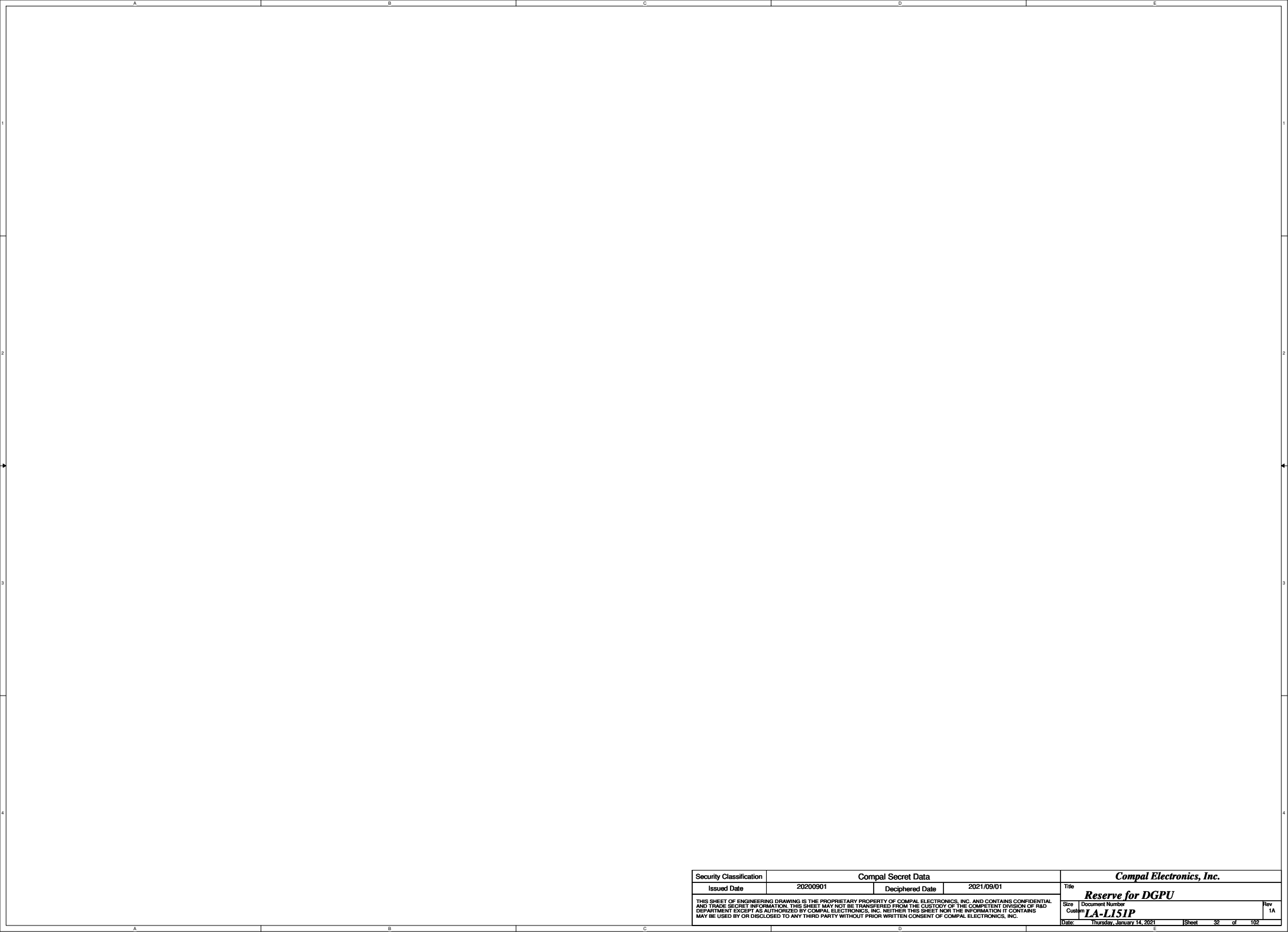
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				Sheet 29 of 102	



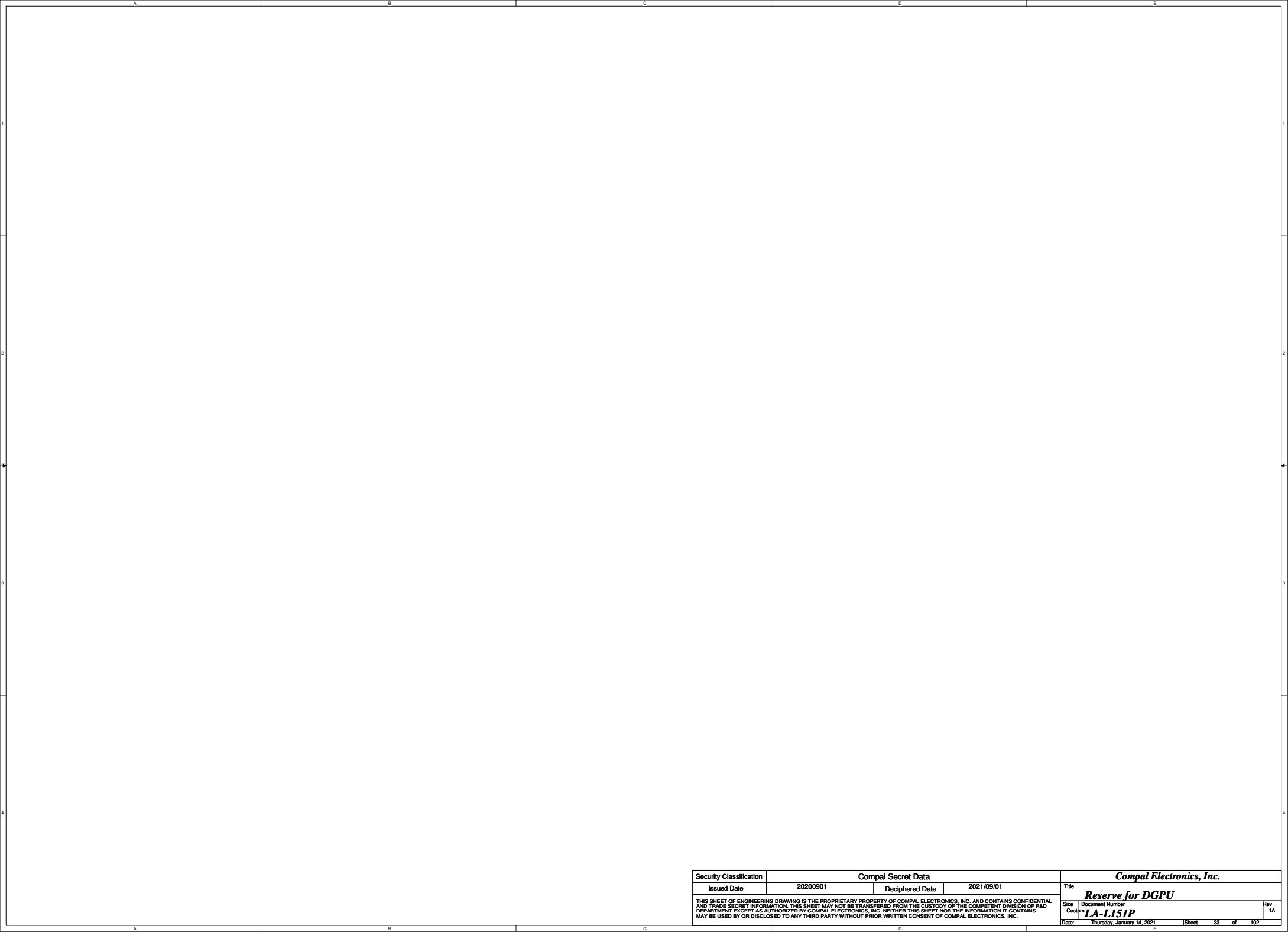
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				Date: Thursday, January 14, 2021	Rev 1A
				Sheet 31 of 102	



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				Customer	LA-L151P	1A
Date: Thursday, January 14, 2021				Sheet	22	of 102



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				Customer	LA-L151P	1A
Date: Thursday, January 14, 2021				Sheet	33	of 102



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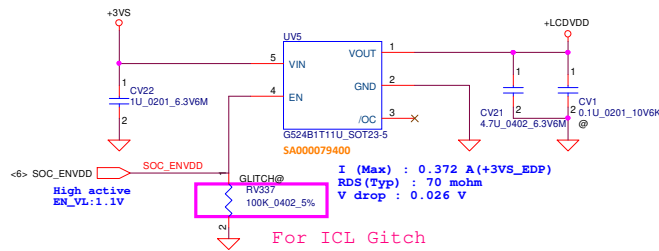
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				Sheet	Rev
				LA-L151P	1A
				Date: Thursday, January 14, 2021	19mm 35 of 102



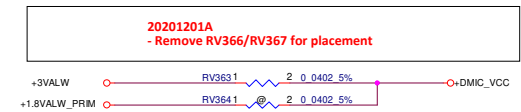
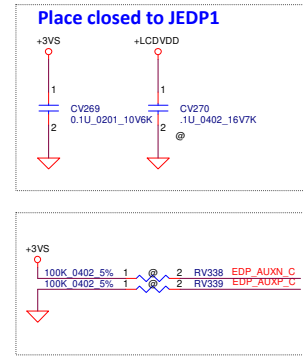
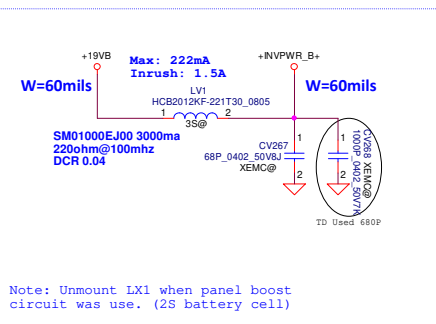
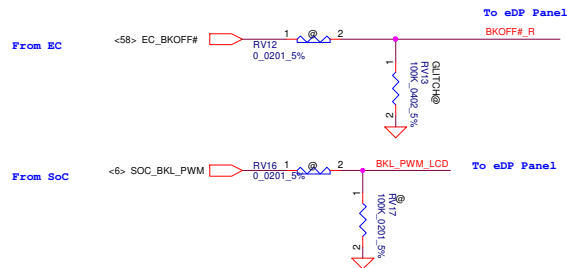
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							LA-L151P		1A	
Date:						Thursday, January 14, 2021		Sheet	36 of 102	



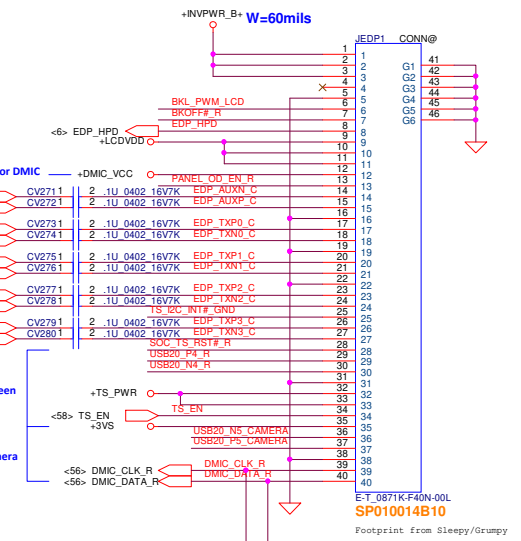
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				LA-L151P	Rev 1A
Date:		Thursday, January 14, 2021		Sheet	37 of 102



Camera

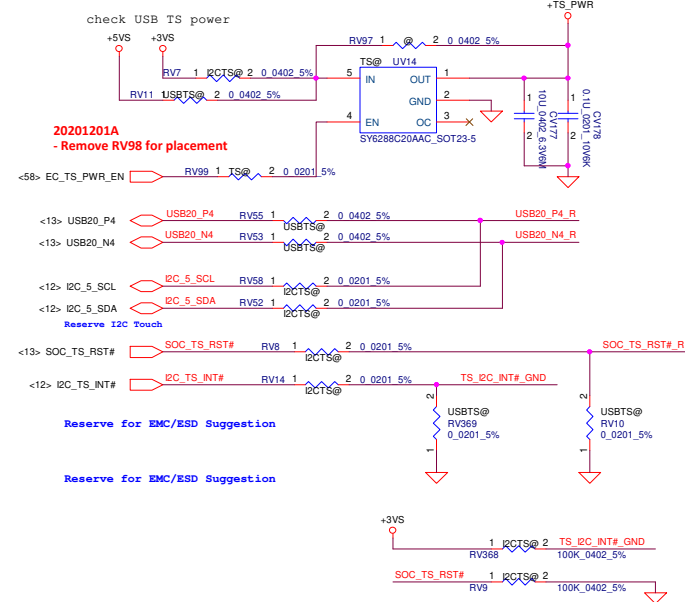


LED PANEL Conn.

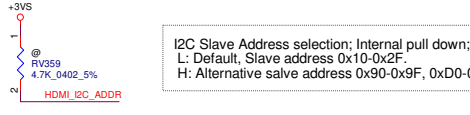
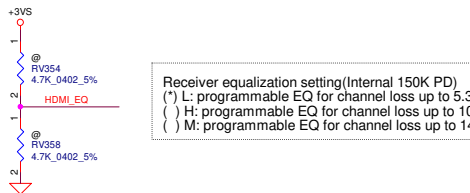
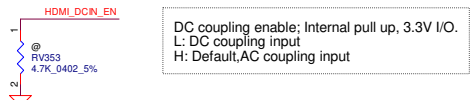
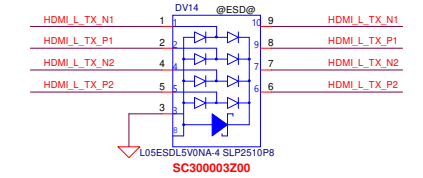
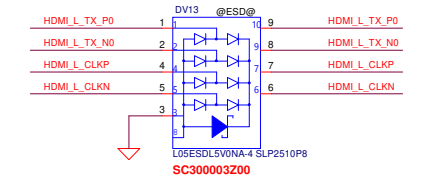
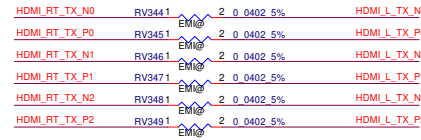
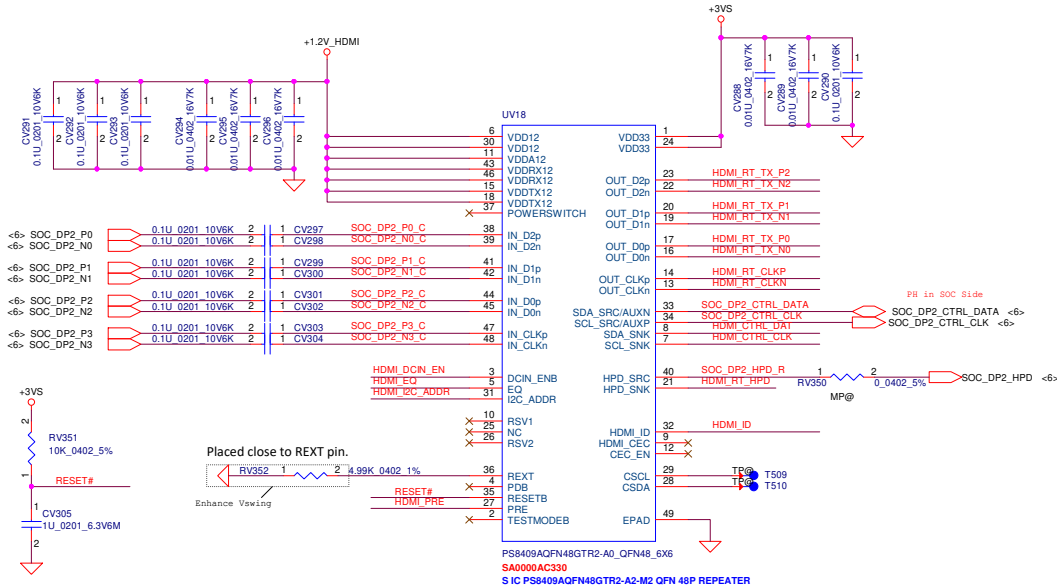
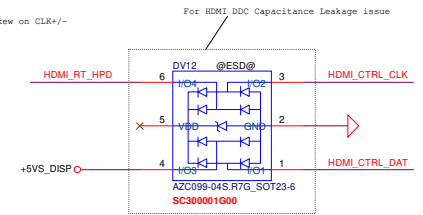
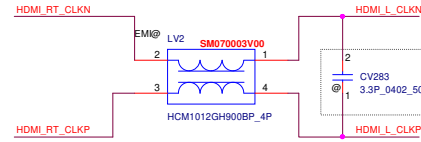
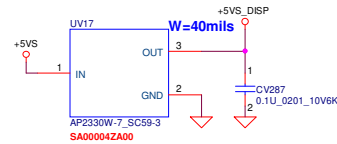
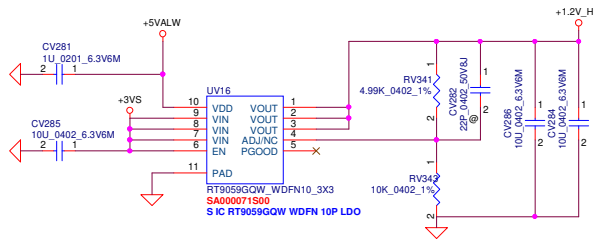


USB/I2C Touch Screen Co-Lay

20200915B
- Add for I2C/USB Touch panel co-lay



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					LA-1151P	
Date:					Thursday, January 14, 2021	Sheet
					38	of 102



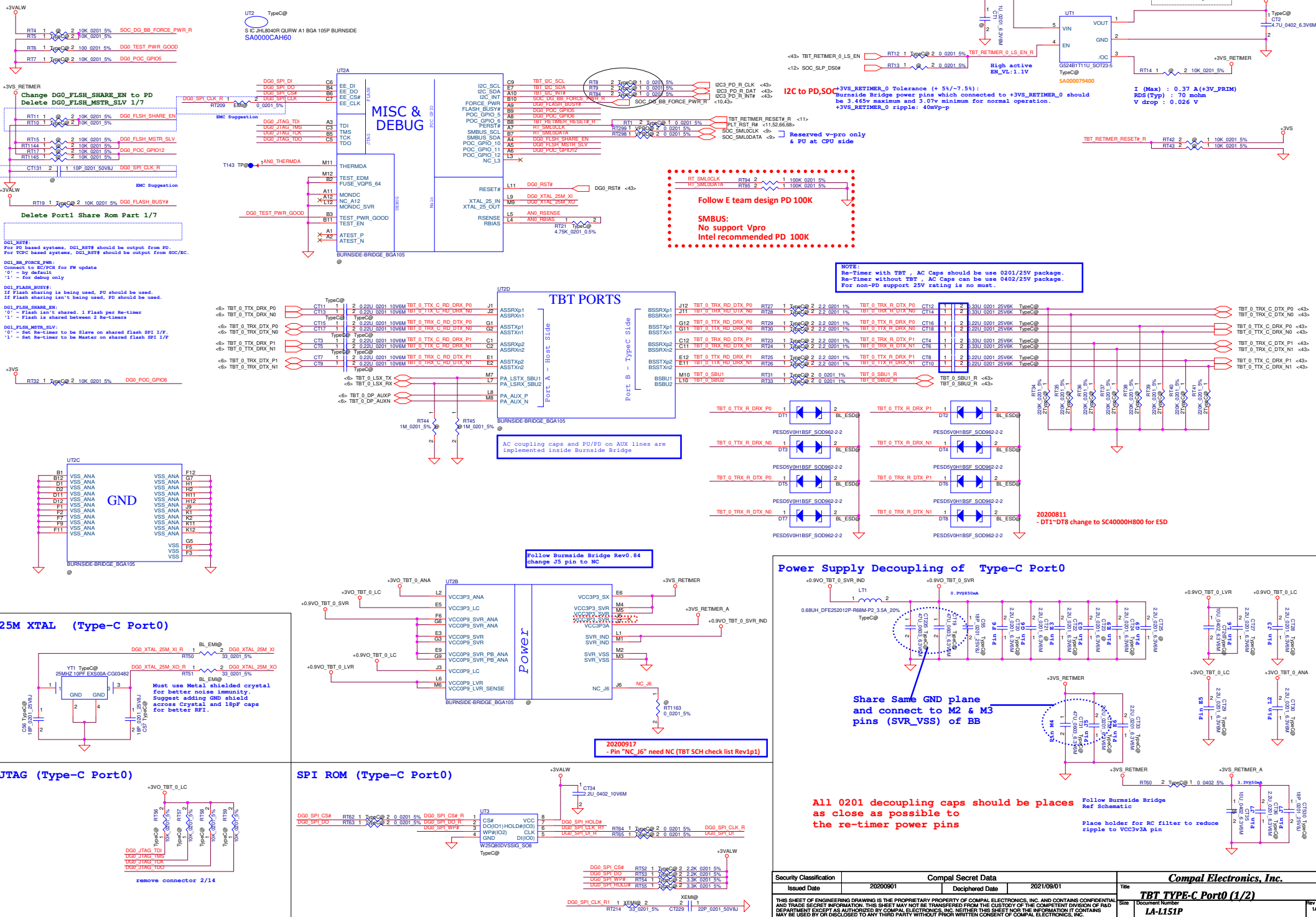


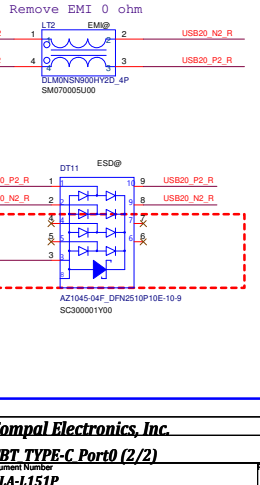
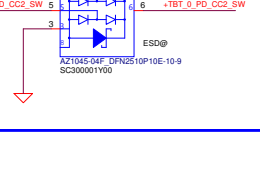
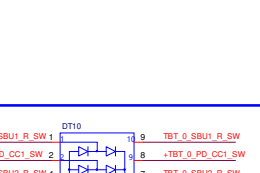
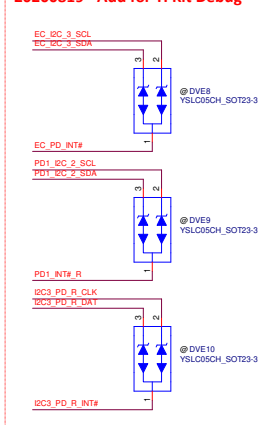
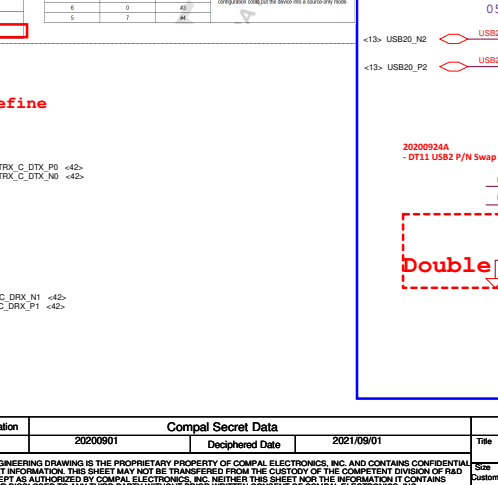
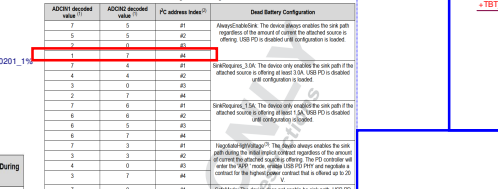
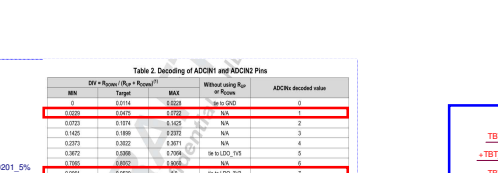
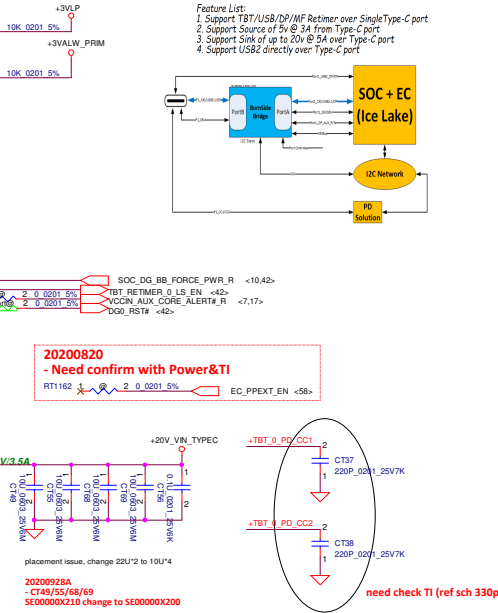
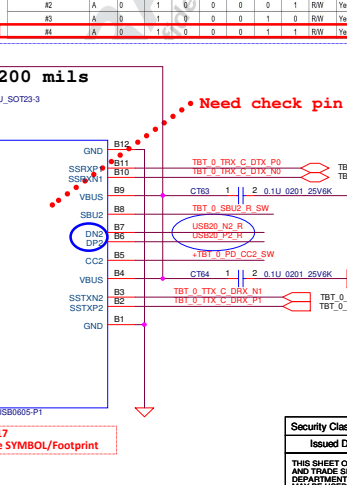
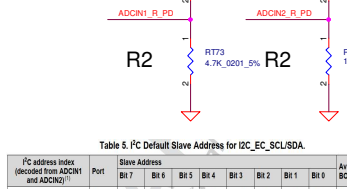
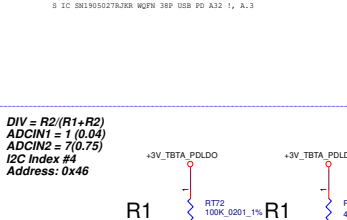
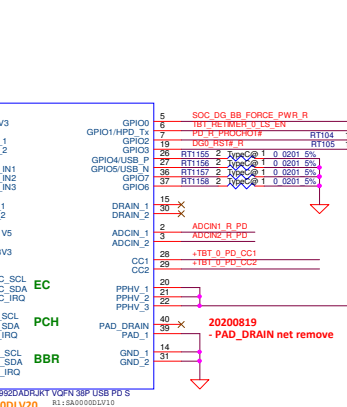
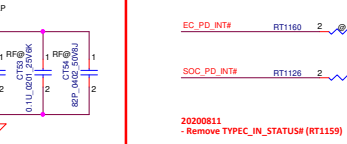
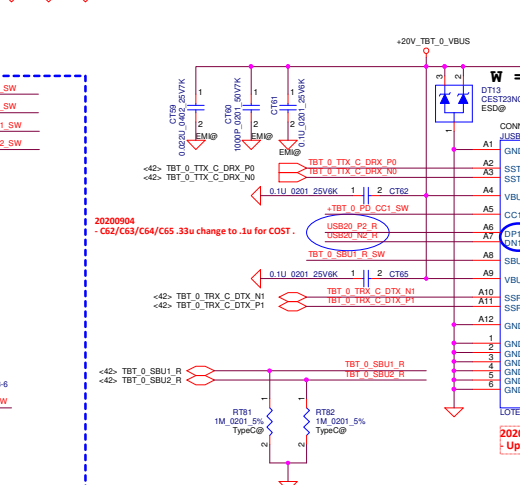
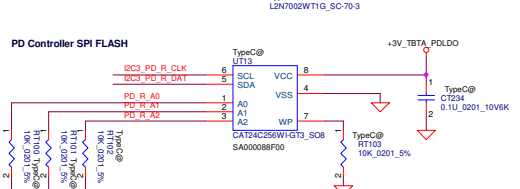
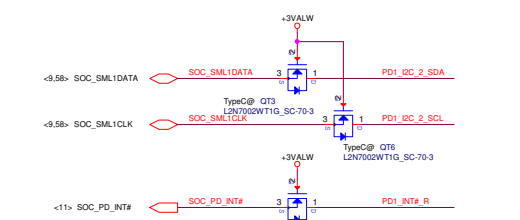
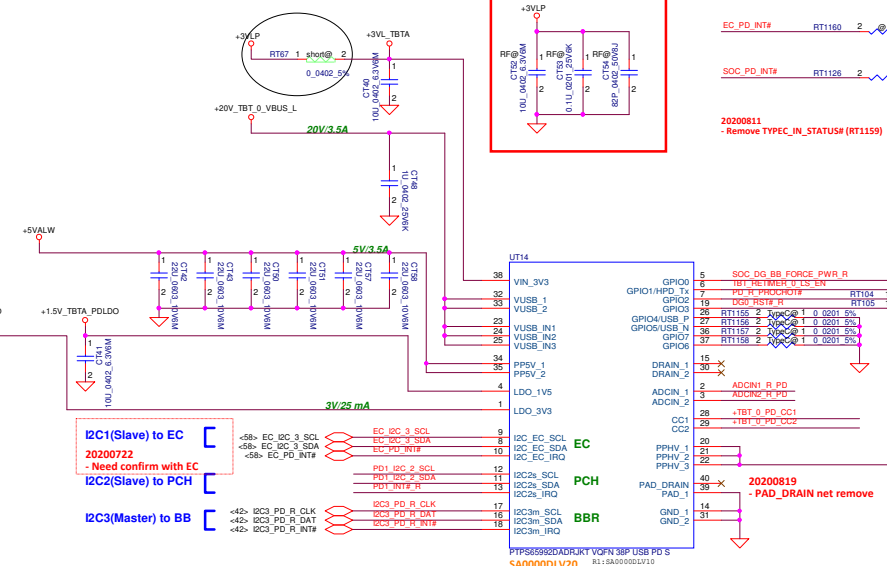
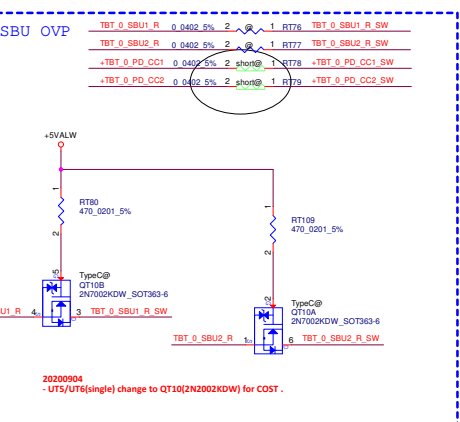
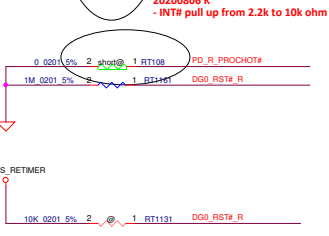
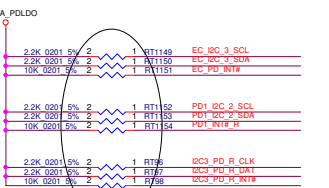
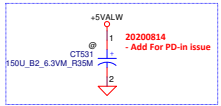
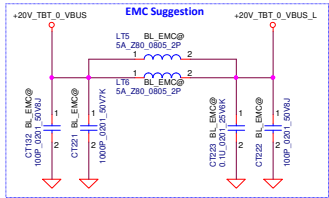
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							LA-L151P			1A	
						Date:		Thursday, January 14, 2021			
						Sheet		40 of 102			



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						Size	Document Number			Rev	
							LA-L151P			1A	
Date:		Thursday, January 14, 2021		Sheet		41		of 102			

MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)





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						Size	Document Number			Rev	
						LA-L151P			1A		
						Date:		Thursday, January 14, 2021		Sheet 45 of 102	

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						Size	Document Number			Rev		
						LA-L151P			1A			
						Date:	Thursday, January 14, 2021		Sheet	46	of	102



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Date:		Thursday, January 14, 2021		Sheet	47 of 102



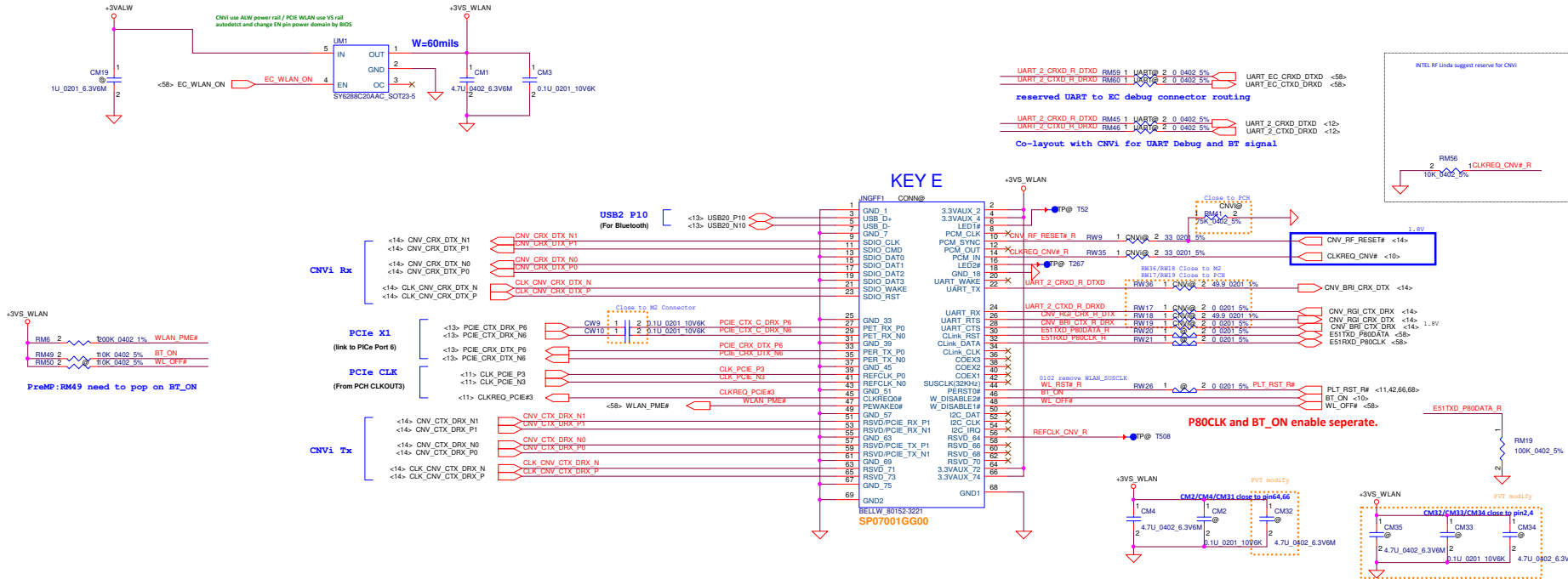
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						Size	Document Number		Rev	
						LA-L151P		1A		
Date:						Thursday, January 14, 2021		Sheet	49 of 102	

MB_USB3.1 TypeC Conn. (Power Path)
- Remove
- TBT4 Change to TI solution

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				LA-L151P	Rev 1A
Date:		Thursday, January 14, 2021		Sheet	50 of 102

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				Size	Document Number
				LA-L151P	
				Rev 1A	
Date:		Thursday, January 14, 2021		Sheet	51 of 102





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						LA-L151P		1A		
Date:						Thursday, January 14, 2021		Sheet	53 of 102	

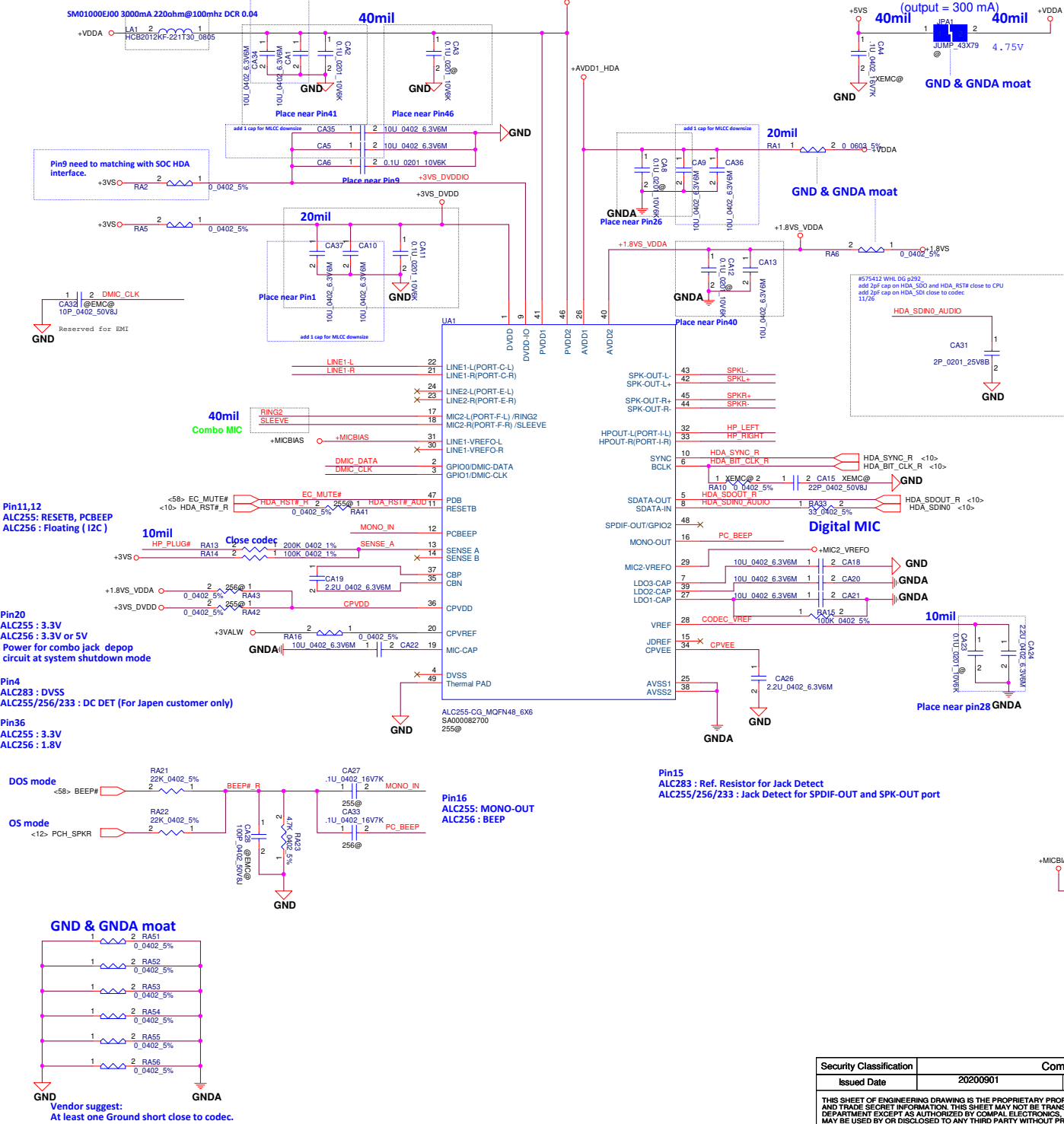


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						Size		Document Number		Rev	
								LA-L151P		1A	
						Date:		Thursday, January 14, 2021			
						Sheet		54 of 102			

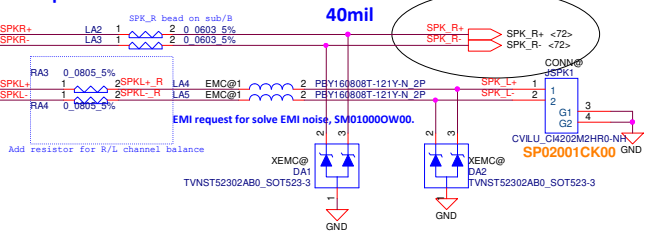


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								LA-L151P		1A	
						Date:		Thursday, January 14, 2021			
						Sheet		55 of 102			

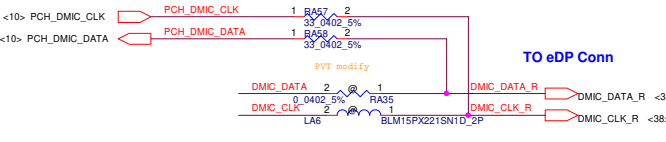
HD Audio Codec



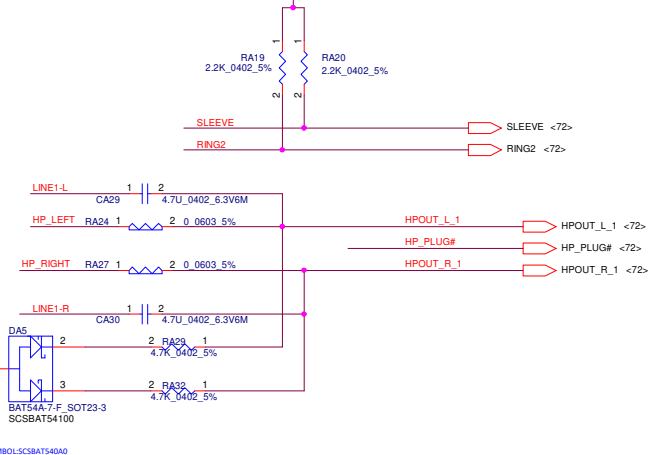
Int. Speaker Conn.



Digital MIC



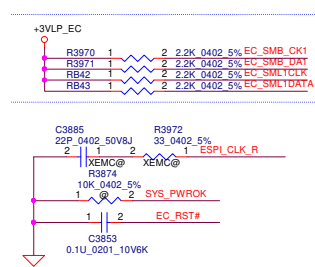
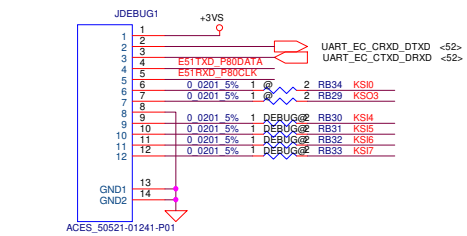
Headphone Out



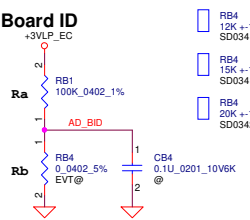
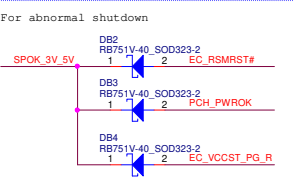
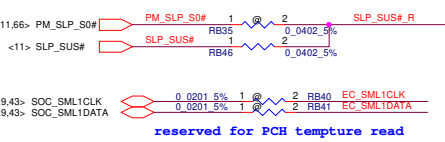
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				Date	Thursday, January 14, 2021
				Sheet	56 of 102



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								LA-L151P		1A	
						Date:		Thursday, January 14, 2021			
						Sheet		57 of 102			

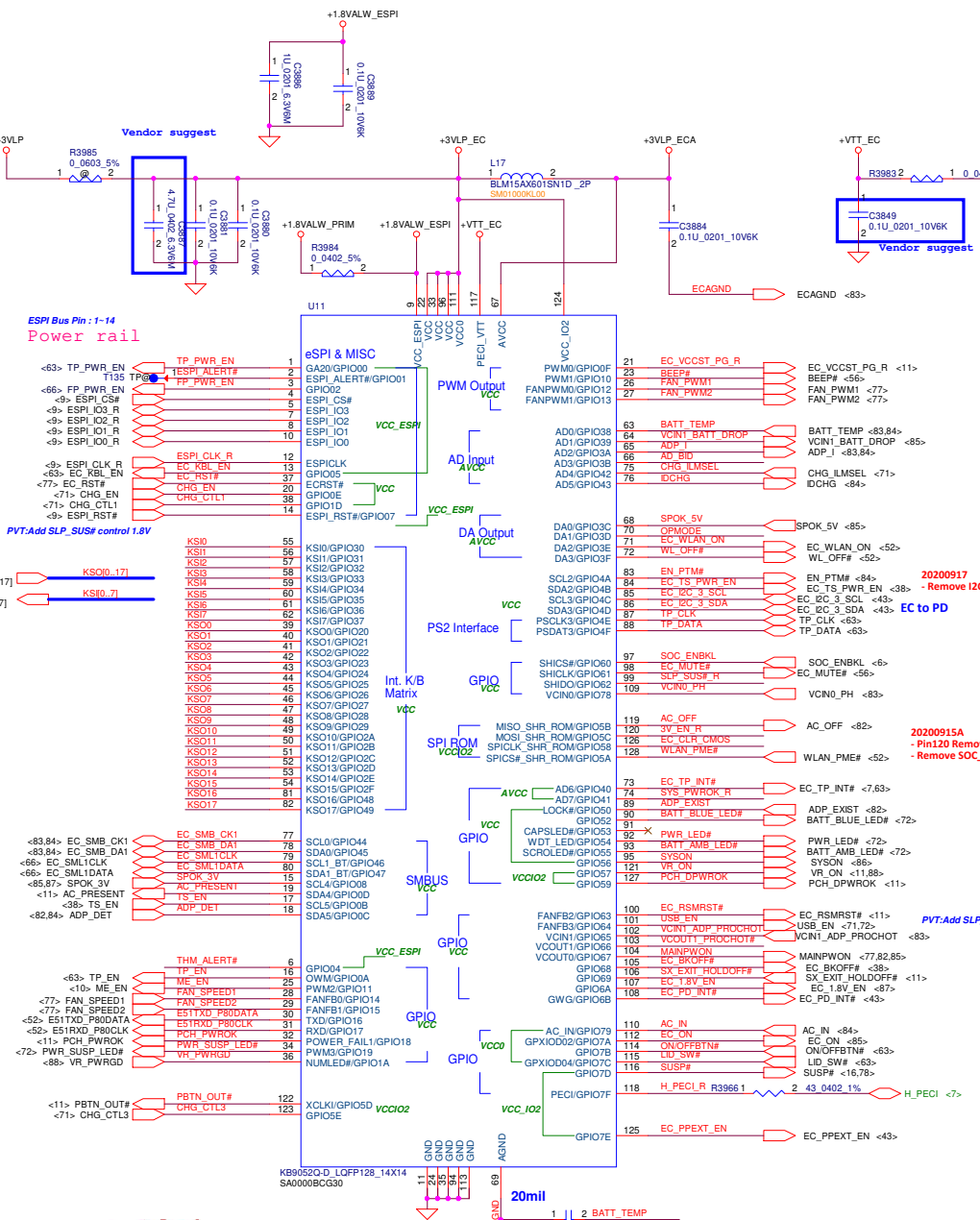


OPMODE (Internal Pull High) :
Pull Up : Intel eSPI Master Attached Flash Sharing Topology
-> For KB9042 / KB9052
Pull Down : Intel Legacy Wire-OR share ROM.
-> For KB9022/9042 Use



Analog Board ID definition, Please see page 3.

20200918A [Remove]
I2C_0_SCL
I2C_0_SDA
SOC_EC_HID_INT#
GPIO4A
GPIO4B
GPIO5A
[Move]
EN_PTM# From GPIO13 to GPIO4A
WLAN_PME# From GPIO15 to GPIO5A
[Add]
FAN_PWM2 (VGA) GPIO13
FAN_SPEED2 (VGA) GPIO15
EC_TS_PWS (Touch panel) GPIO4B

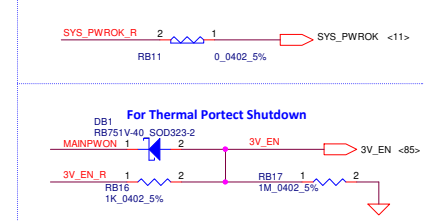
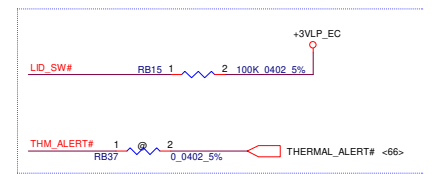
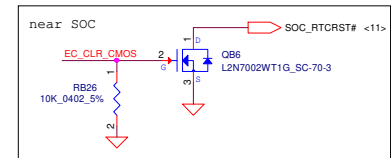


KB9052-D LGFP128_14X14 SA000BCG30

IO pin groups v.s Power planes:

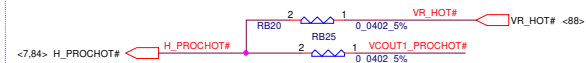
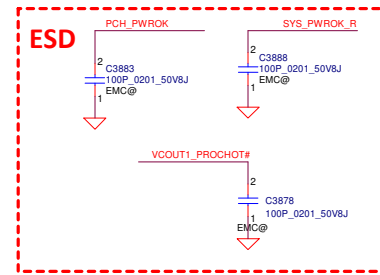
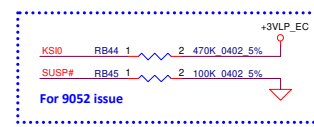
Power plane	Voltage	Pin#	Output Pin Power Rail	Input Pin VIH/VIL
VCC0	3.3V~2.0V(min) for PLC operation and data retention	110, 112, 114, 115	Push-pull @ VCC0 Open-Drain up to 5V	ref. to VCC0
VCC	3.3V only	15-43 77-109	Push-pull @ VCC Open-Drain up to 5V	ref. to VCC
VCC_ESPI	1.8V	1-14	Push-pull @ VCC_ESPI Open-Drain up to VCC_ESPI	ref. to VCC_ESPI
AVCC	3.3V only	63-76 (102, 109)	Push-pull @ AVCC Open-Drain up to 5V	ref. to AVCC
VCC_I02	1.8V or 3.3V	116, 118-128	Push-pull @ VCC_I02 Open-Drain up to 5V	ref. to VCC_I02
PECL_Vtt	External applied Vtt	117		

Note :
pin-109 (VCIN0) can be programmable internally connected to ADC ch8 (ADC8) and pin-102 (VCINT) to ch9 (ADC9) by setting ADEN2[5:4]. If so, the voltage level on these two pins should not be higher than AVCC to prevent leakage.



20200917
- Remove I2C_0, PD(TI) is not used.
EC to PD

20200915A
- Pin120 Remove PD_USB1_SRC_HI_ILUM for PD TI
- Remove SOC_EC_HID_INT# (TI PD not used)



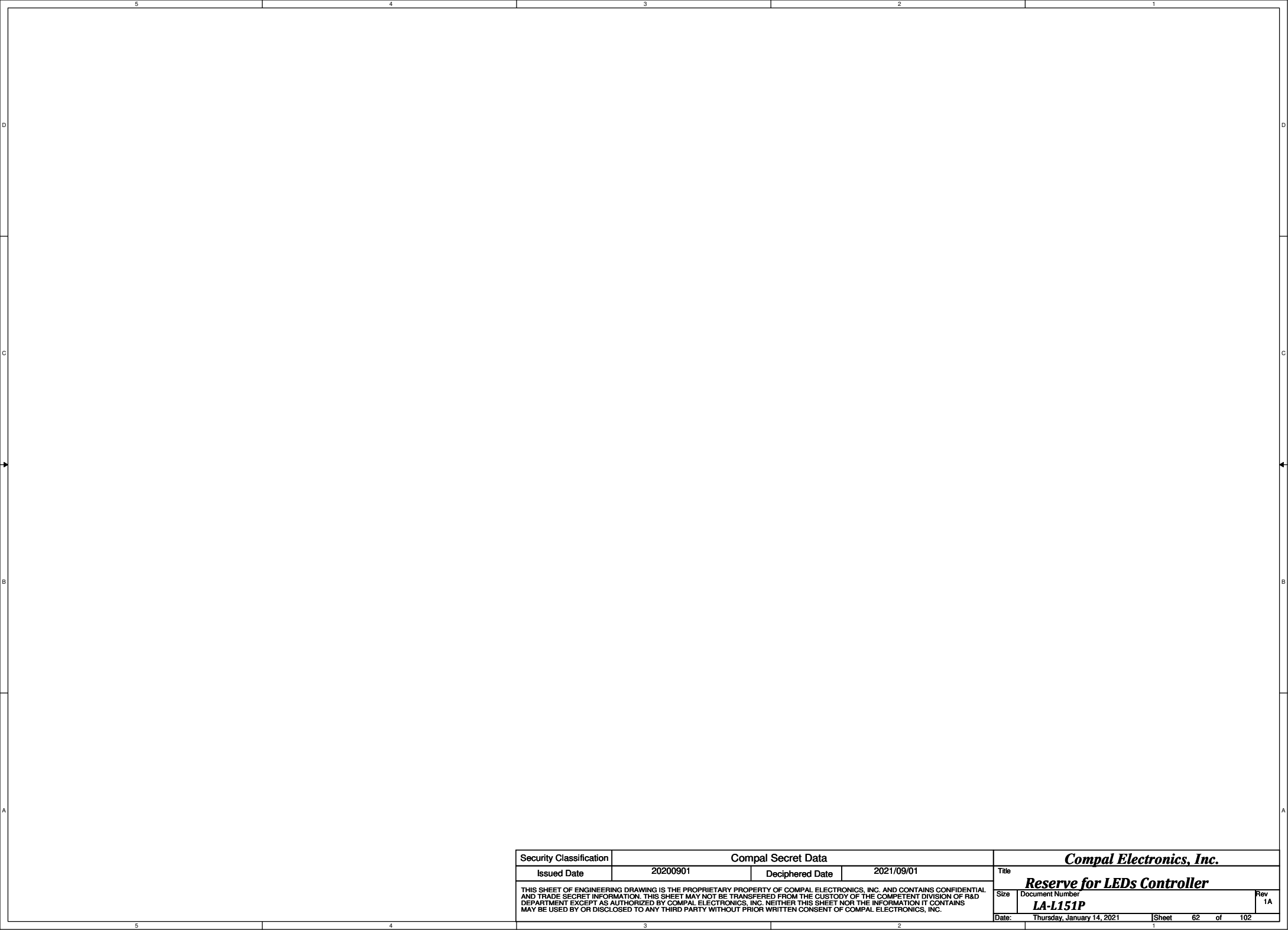


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Date:						Thursday, January 14, 2021		Sheet	59 of 102	

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					LA-L151P	1A	
				Date:	Thursday, January 14, 2021	Sheet	60 of 102

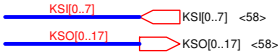


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						Size		Document Number		Rev	
								LA-L151P		1A	
						Date:		Thursday, January 14, 2021		Sheet 61 of 102	



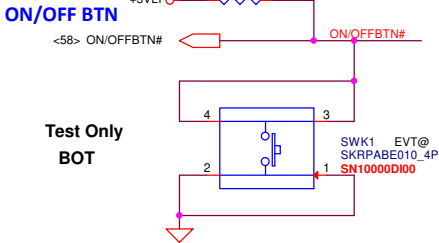
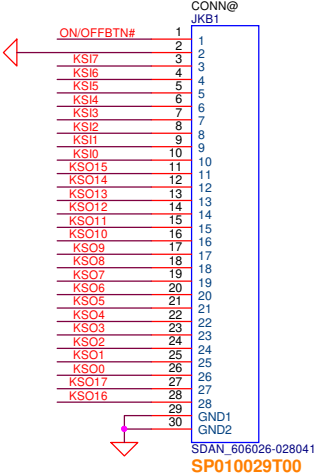
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							LA-L151P			1A	
						Date:		Thursday, January 14, 2021			
						Sheet		62 of 102			

KB Conn.

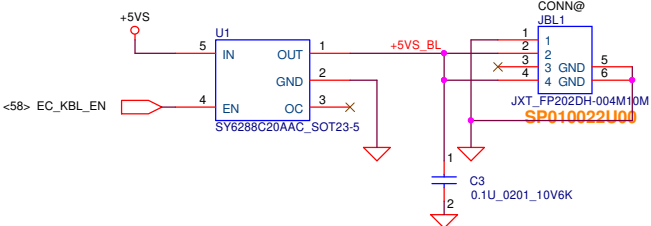


20200918A

- Modify pin define

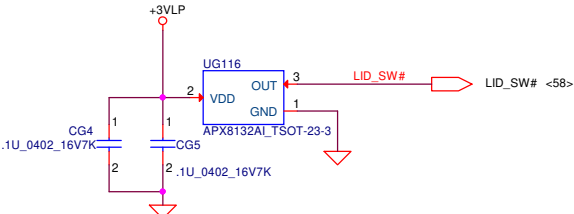


KB BackLight

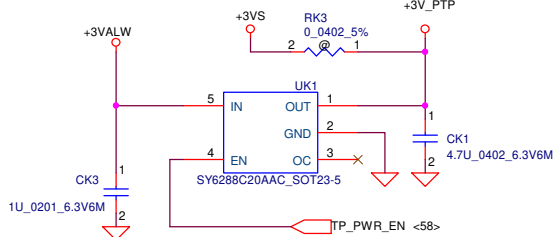


Lid Switch

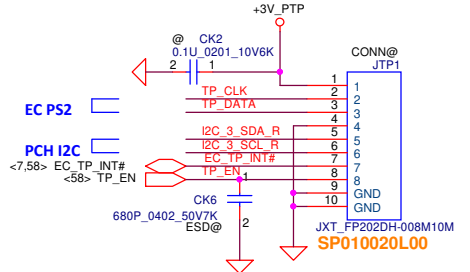
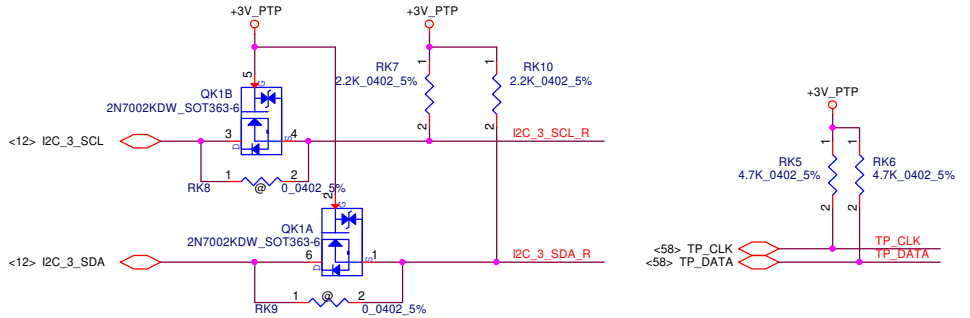
20200914
- Change to ON MB



TP/B Conn.



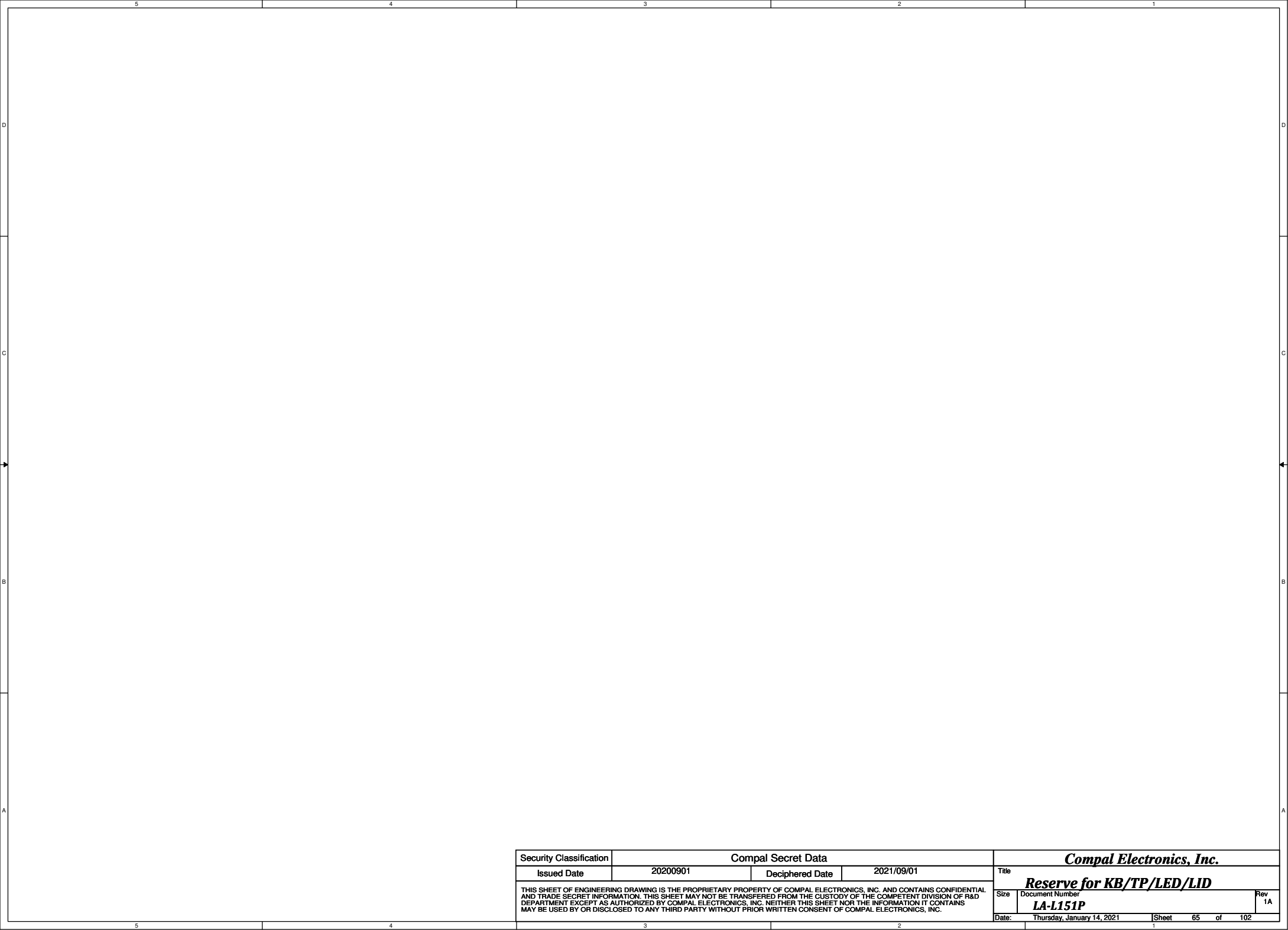
TP_PWR_EN follow SYSON behavior



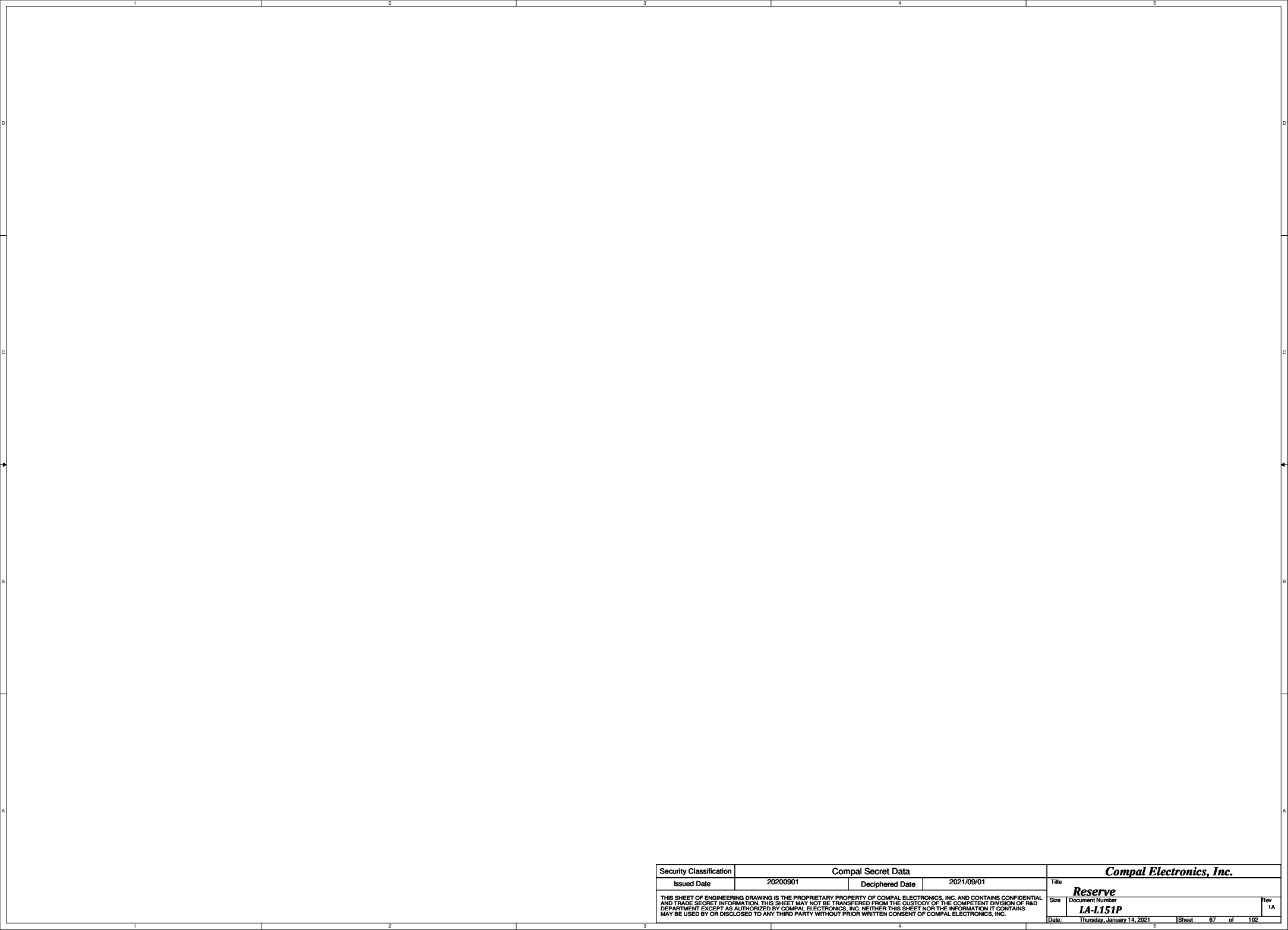
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				Custom	LA-L151P	1A			
				Date:	Thursday, January 14, 2021	Sheet	63	of	102



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							LA-L151P			1A	
Date:		Thursday, January 14, 2021			Sheet		64	of	102		

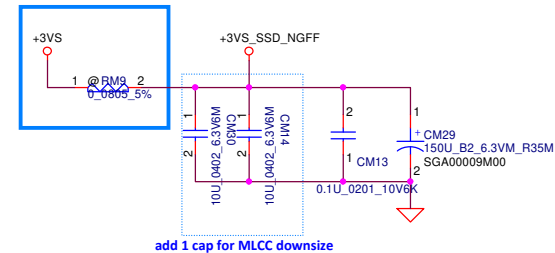


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						Size		Document Number		Rev	
								LA-L151P		1A	
Date:		Thursday, January 14, 2021				Sheet		65 of 102			



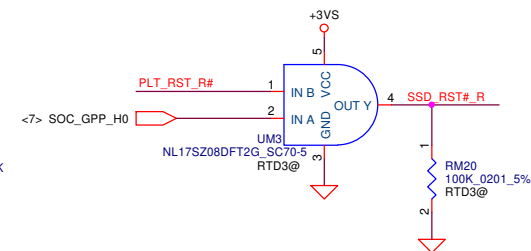
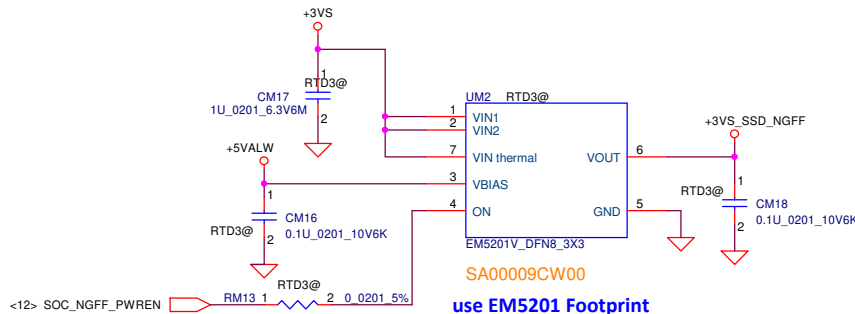
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				Date:	Thursday, January 14, 2021	Rev 1A
				Sheet	57	of 102

M.2 SSD

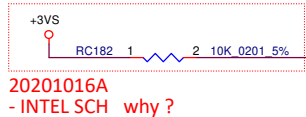
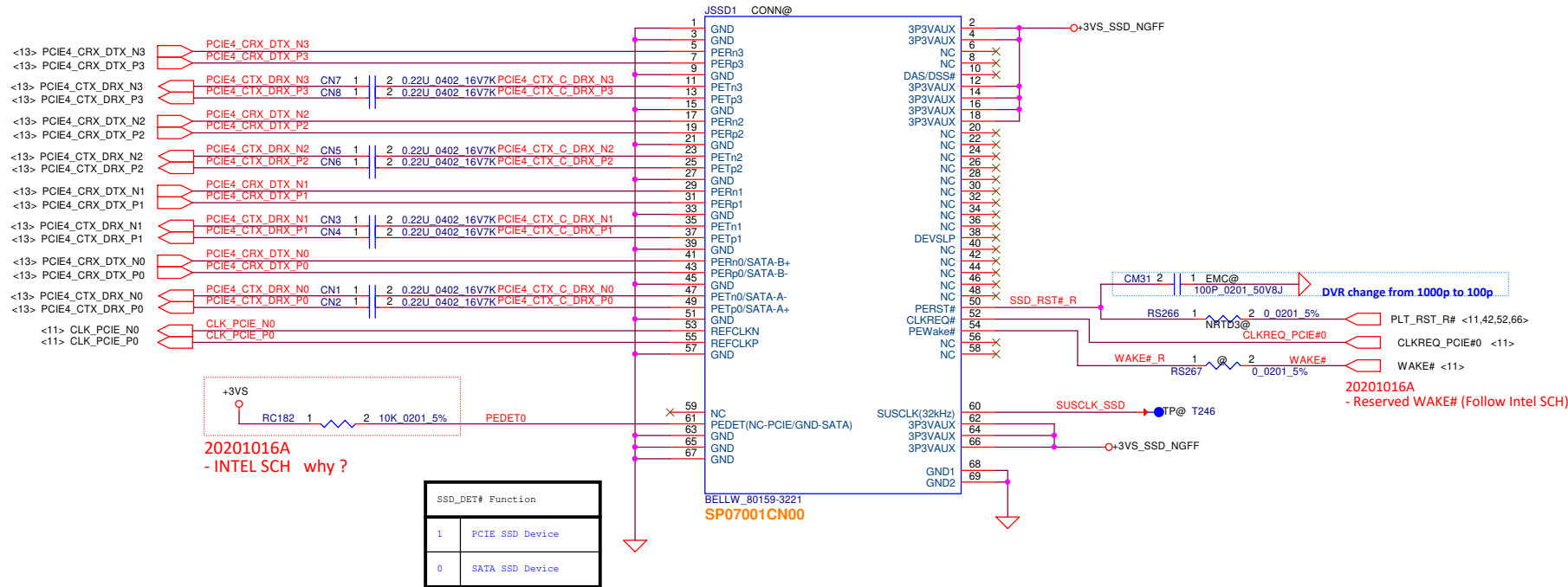


SSD1 (Gen3)

reserve for RTD3



KEY M



20201016A
- INTEL SCH why ?

SSD_DET# Function	
1	PCIE SSD Device
0	SATA SSD Device

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						LA-L151P		
Date:			Thursday, January 14, 2021			Sheet 68 of 102		
						Rev 1A		

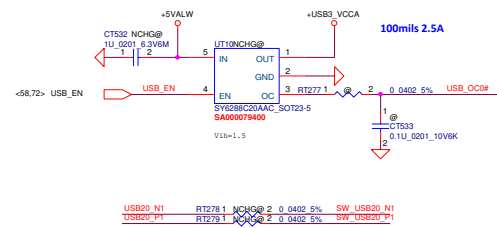


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		Size	Document Number						Rev
		LA-L151P						1A	
		Date:		Thursday, January 14, 2021		Sheet		69	of 102

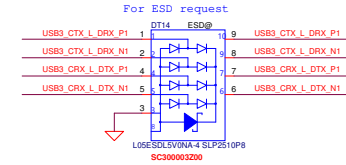
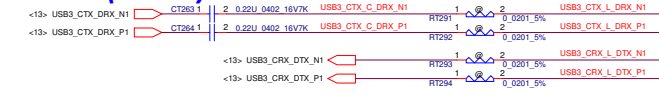
+3VS TO +3VS_CARD

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			Date:	Thursday, January 14, 2021	1A
			Sheet	70	of 102

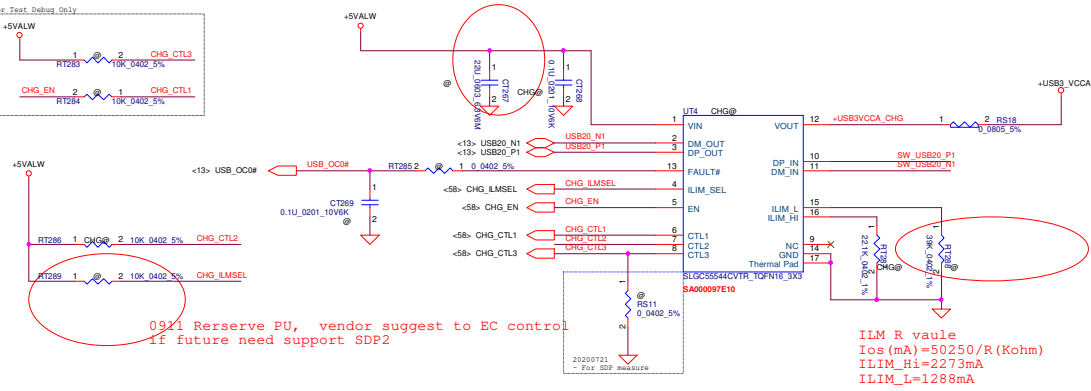
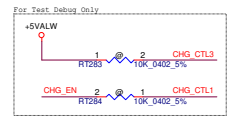
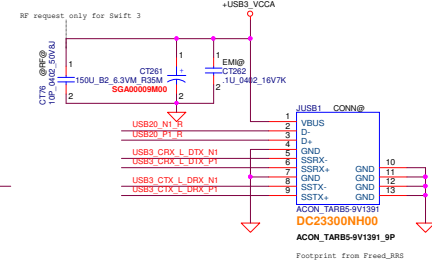
Non-Charger Co-lay



USB3.0 (Port 1)



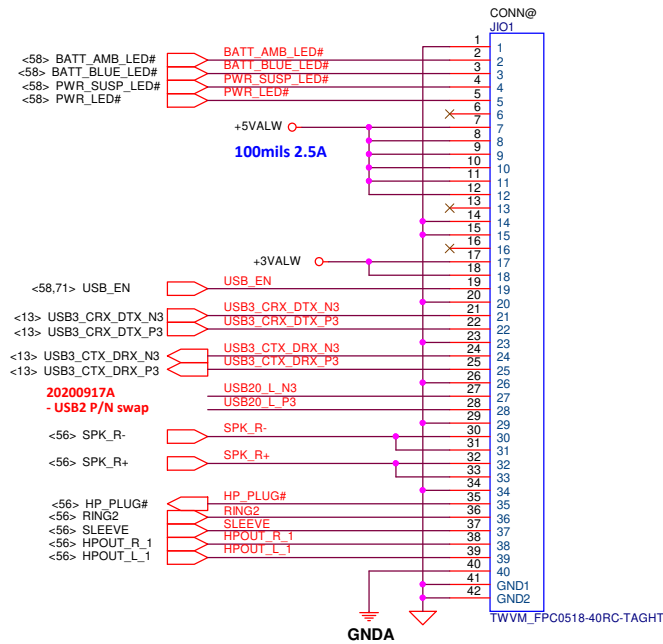
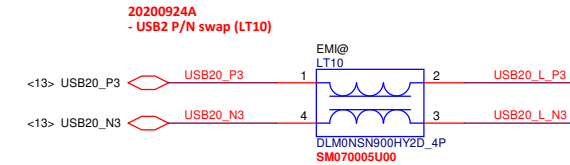
USB3.0 Conn.



USB Host Charger Truth Table

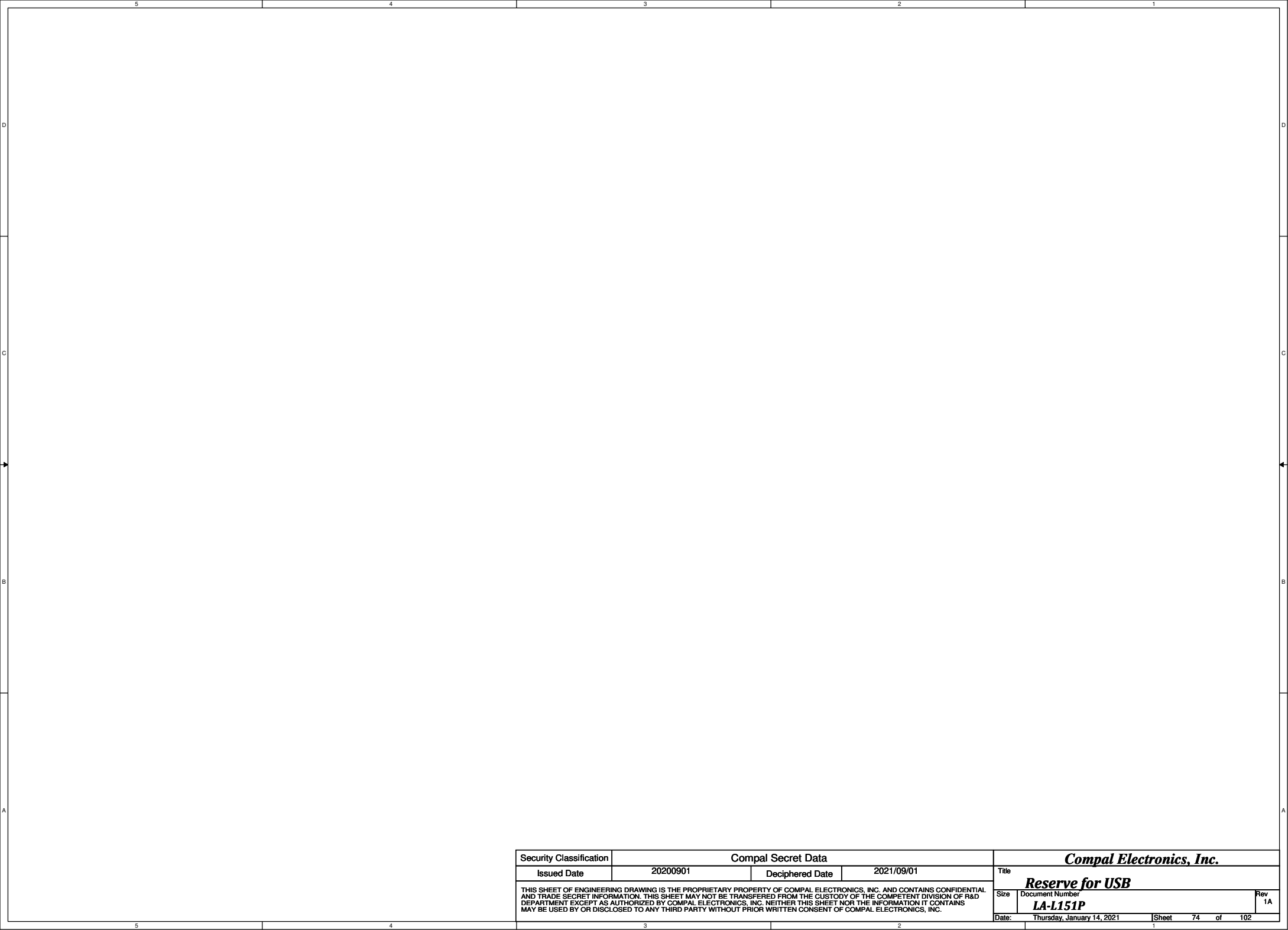
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

IO/B_USB3_HP Jack



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		LA-LI51P			1A
Date:		Thursday, January 14, 2021		Sheet	72 of 102

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				LA-L151P		
Date: Thursday, January 14, 2021				Sheet	73	of 102



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						Size		Document Number		Rev	
								LA-L151P		1A	
						Date:		Thursday, January 14, 2021			
						Sheet		74 of 102			

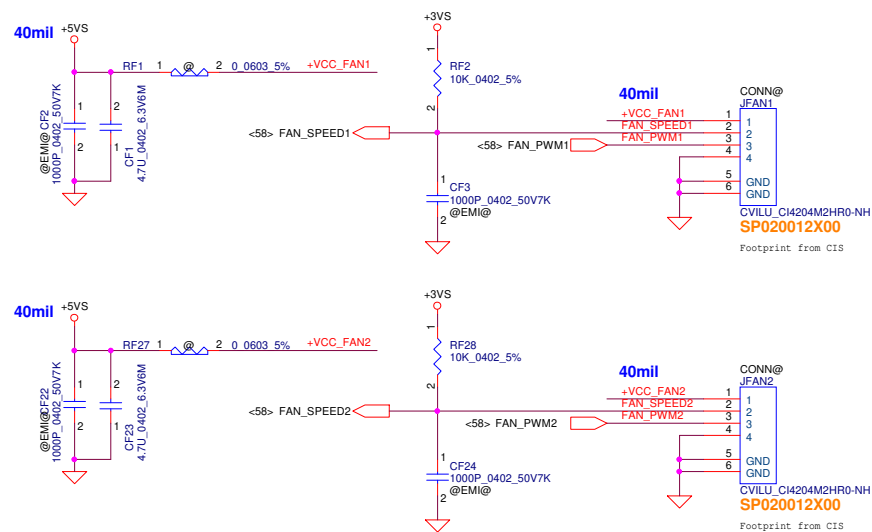


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						Size	Document Number			Rev	
						LA-L151P			1A		
Date:						Thursday, January 14, 2021		Sheet	75 of 102		

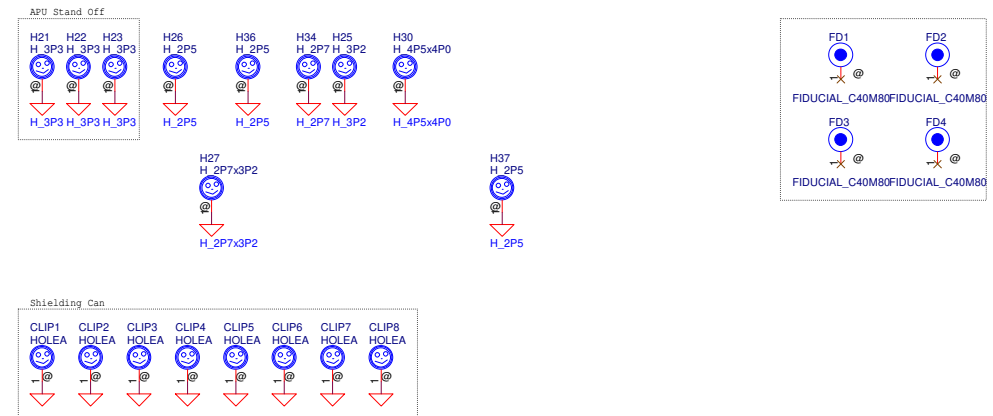


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						Size	Document Number		Rev	
							LA-L151P		1A	
Date:						Thursday, January 14, 2021		Sheet	76 of 102	

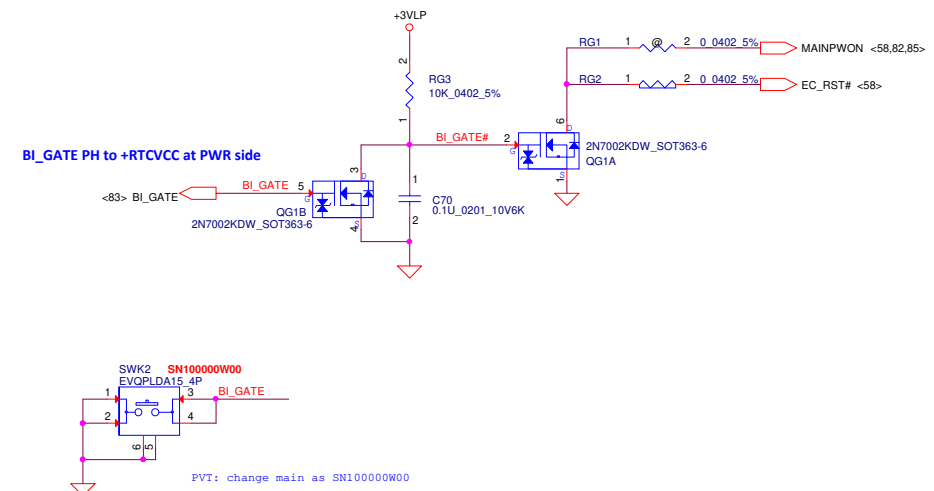
FAN Conn



Screw Hole



Reset Circuit



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				Customer	Rev 1A
				Date:	Thursday, January 14, 2021
				Sheet	77 of 102

+3VALW TO +3VS

+1.8VALW_PRIM TO +1.8VS

+5VALW TO +5VS

DIS (1.8VSDGPU_AON and +1.8VSDGPU_MAIN), remove

20200915B 20200917
- Total 14 pcs - Remove ALL

ME Keyboard Braket Support

Place below component at Keyboard support white paint area.

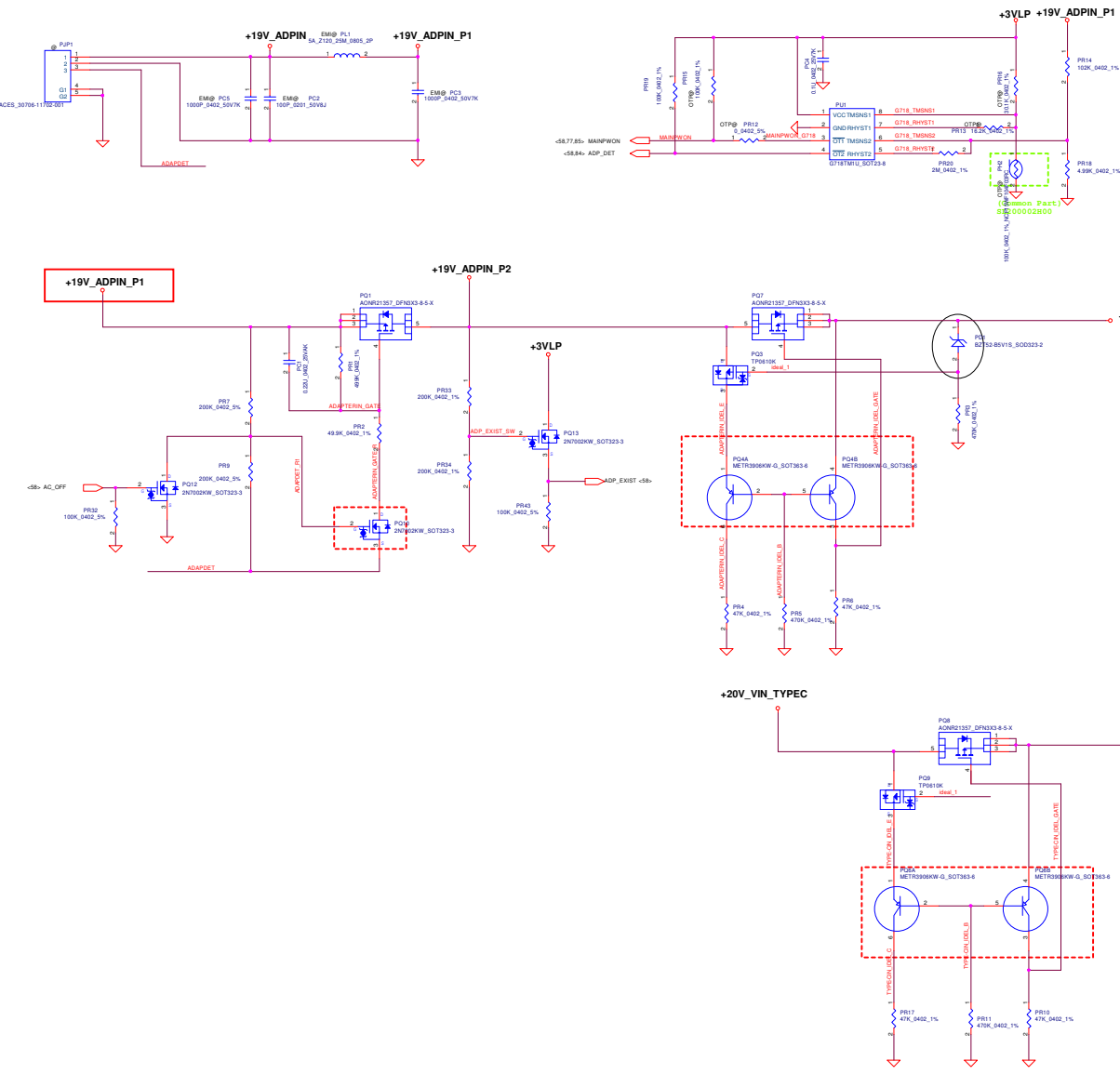
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					LA-1151P	1A
				Date:	Thursday, January 14, 2021	Sheet 79 of 102



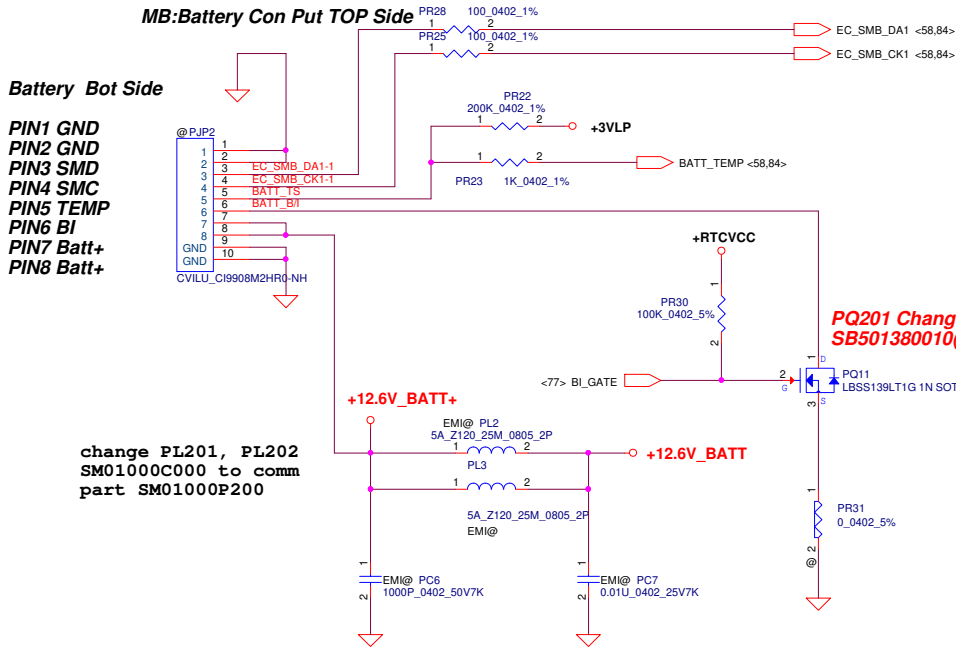
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				LA-L151P	Rev 1A
Date:		Thursday, January 14, 2021		Sheet	80 of 102

PWR-Reserve Page

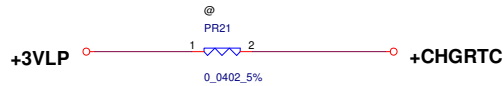
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				B	LA-L151P	1.0
Date:	Thursday, January 14, 2021			Sheet	81	of 102



EC控制 OFF代表被智控更新



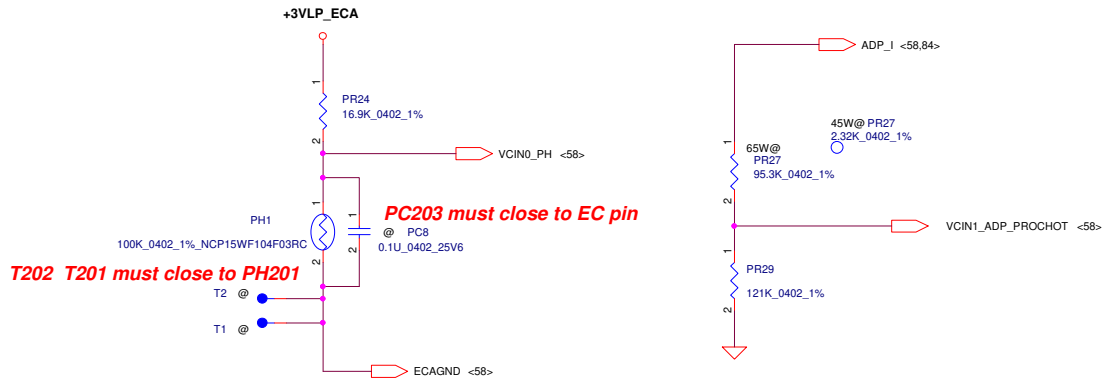
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

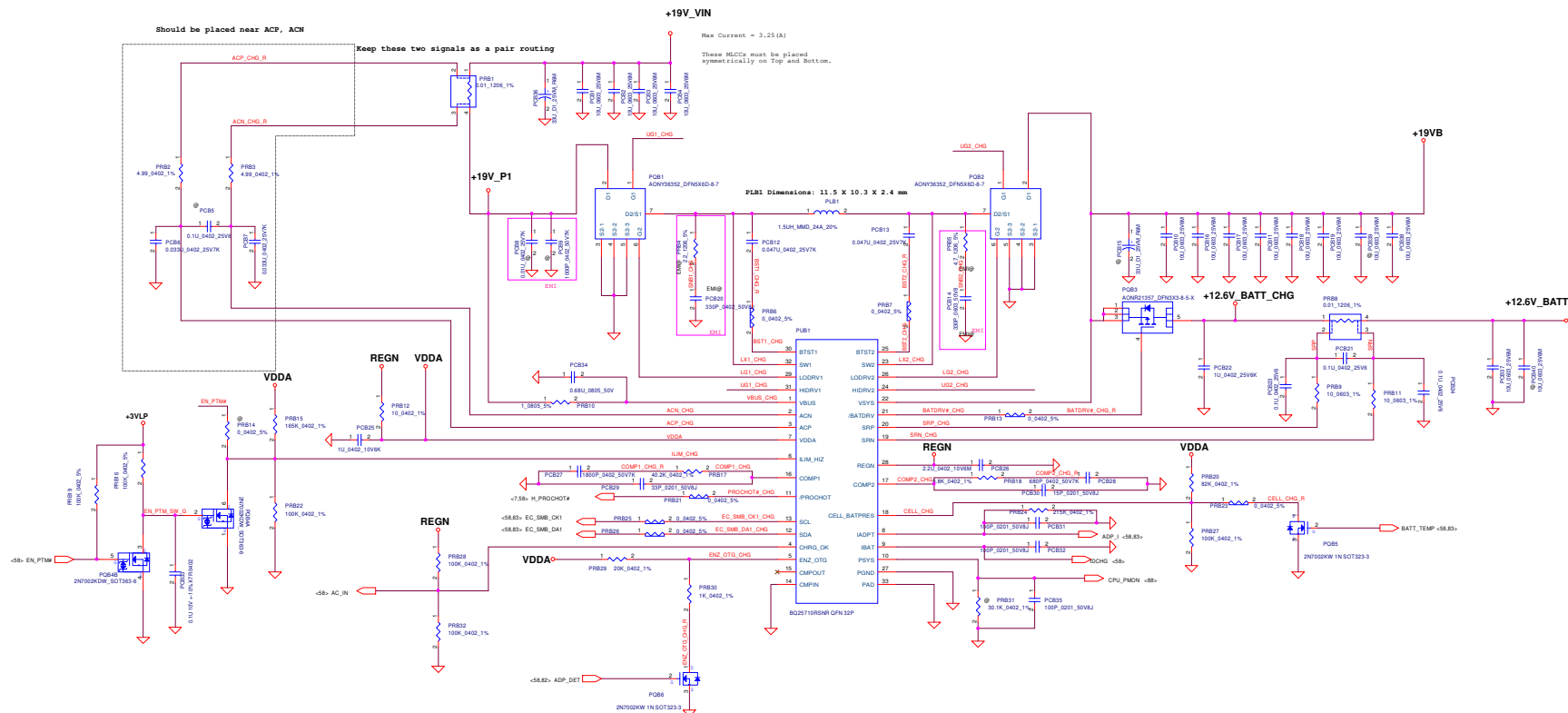


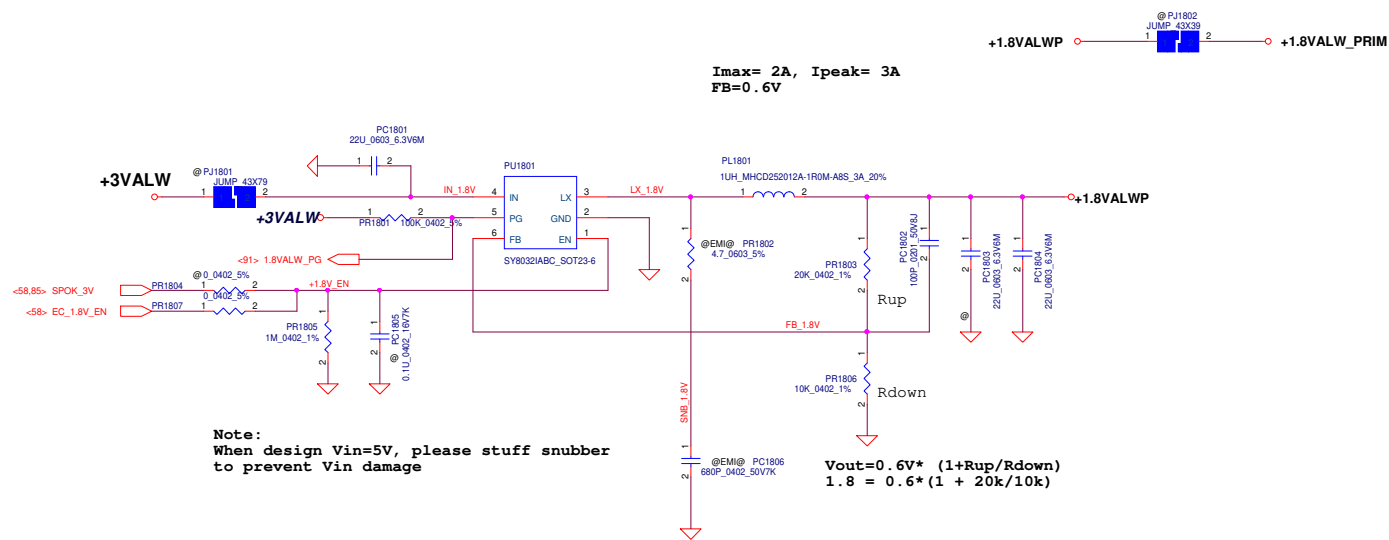
2016/11/16 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR206 2.32K ohm	58.5W, 1V	Active=recovery
65W PR206 7.87K ohm	84.5W, 1V	Active=recovery
90W PR20K ohm	__W, __V	Active=recovery
PH1	2V	1V

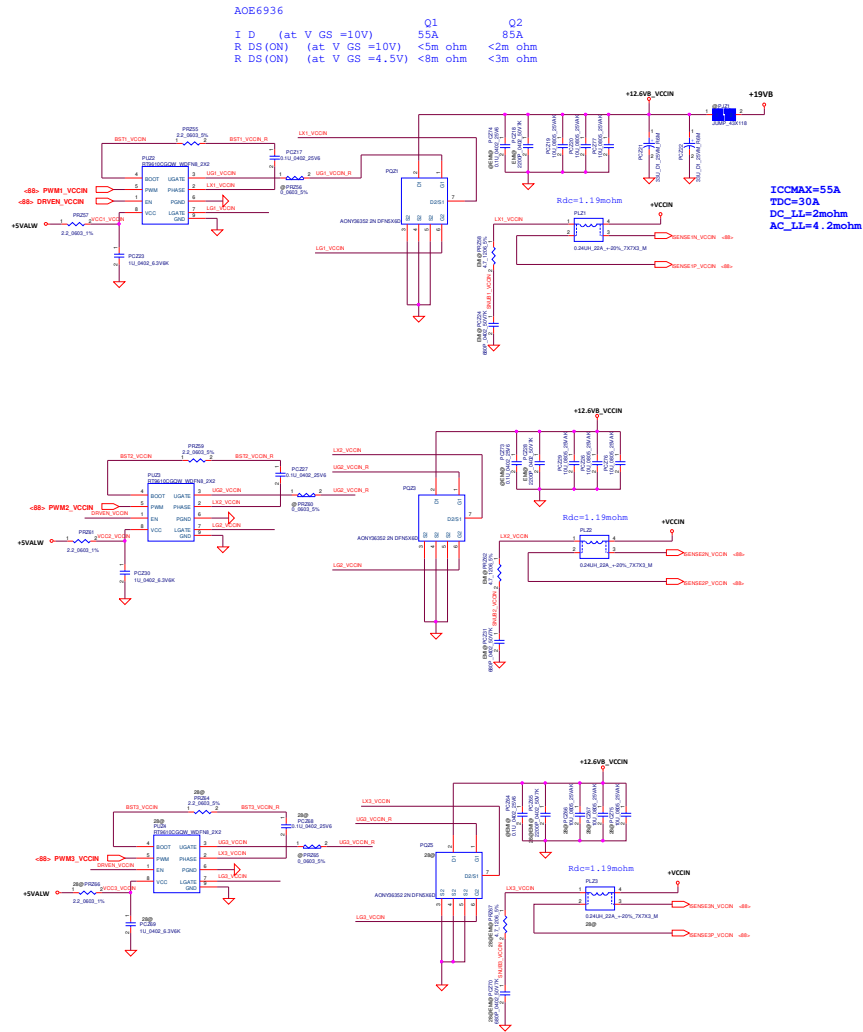
PH1 under CPU bottom side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

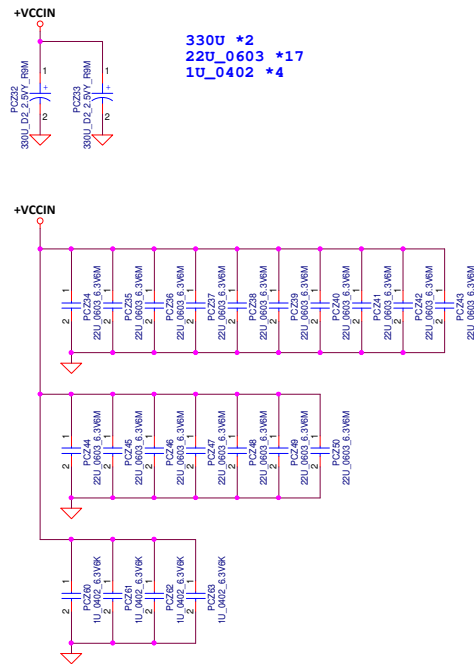






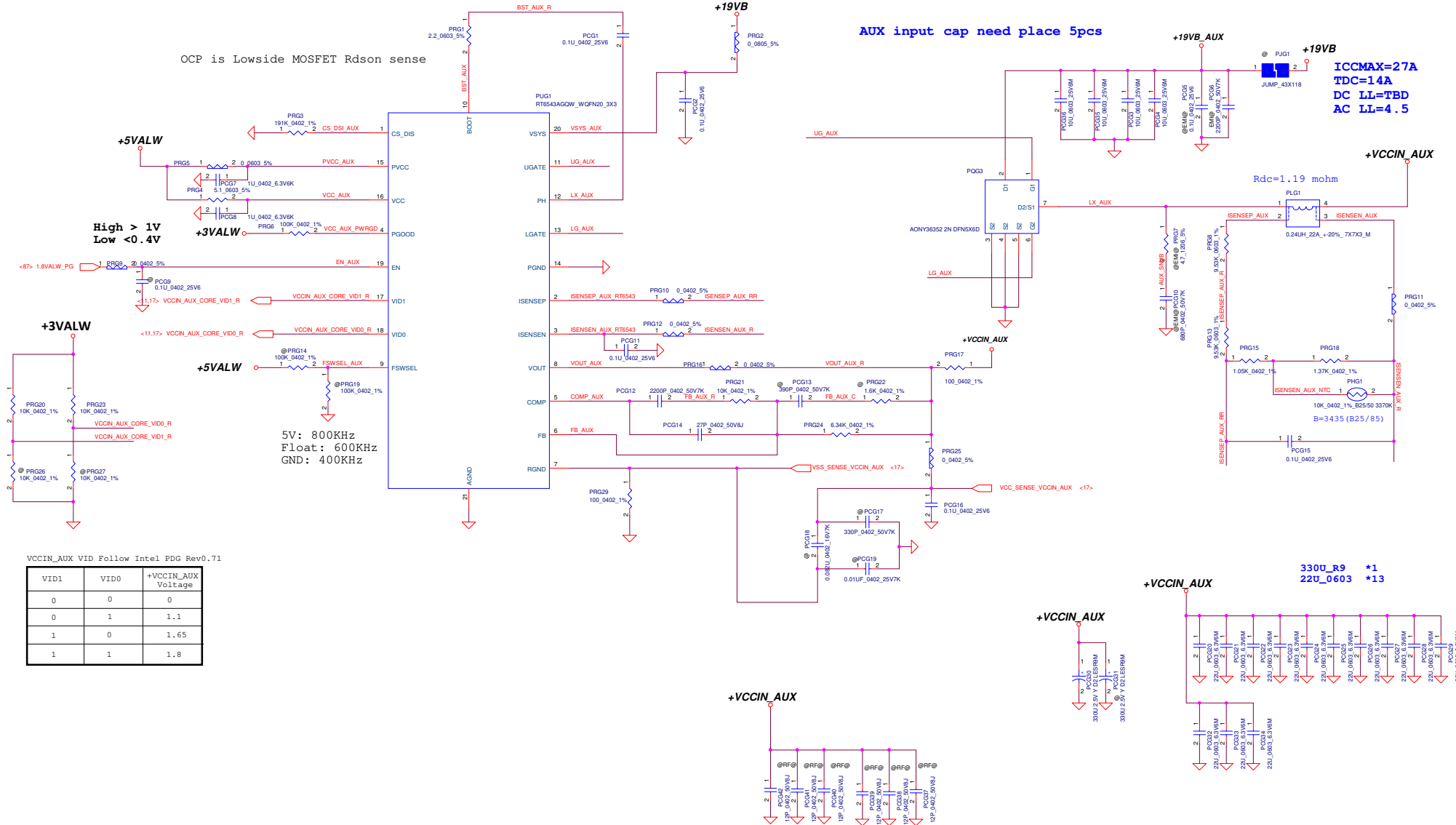
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				Date: Thursday, January 14, 2021	Rev 1.0
				Sheet 87 of 102	





Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion

OCP is Lowside MOSFET Rdson sense



PWR-Reserve Page

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				B	LA-L151P	1.0
Date:				Thursday, January 14, 2021		Sheet 92 of 102

PWR-Reserve Page

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				Size	Document Number
				B	LA-L151P
Date:				Thursday, January 14, 2021	Sheet 93 of 102

PWR-Reserve Page

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				B	LA-L151P	1.0
Date:				Thursday, January 14, 2021		Sheet 94 of 102

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				B	LA-L151P	1.0
Date:				Thursday, January 14, 2021		Sheet 95 of 102

PWR-Reserve Page

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				B	LA-L151P	1.0
Date:	Thursday, January 14, 2021			Sheet	96	of 102

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				B	LA-L151P	1.0
Date:	Thursday, January 14, 2021			Sheet	97	of 102

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				B	LA-L151P	1.0
Date:	Thursday, January 14, 2021			Sheet	98	of 102

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				B	LA-L151P	1.0
Date:				Thursday, January 14, 2021		Sheet 99 of 102

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				B	LA-L151P	1.0
Date:				Thursday, January 14, 2021		Sheet 100 of 102

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		CPU_CORE transient test for GH6UT		P088	PRZ79 change to SD034133280 PRZ76 change to SD034137280 PRZ83 change to SD034287280 PRZ78 change to SD034634180 PRZ33 change to SD034787180	20201214	PVT2
02		Sourcer request		P084	PCB31,PCB32,PCB35,PC1802 change to SE00000SE00. PCB30 change to SE00000TD00	20201214	PVT2
03		Design change		P088	Design reserve PRZ49	20201214	PVT2
06							
07							
08							
09							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							

Version change list (P.I.R. List)					Page 1 of 2 for HW	
Item	Page	Title	Date	Issue Description	Solution Description	Phase Rev.
1	11-13-68	SSD	1016A	PCB Rev 0.2 PCIe change to GEN4	- PCIe change to GEN4 - CLK change to Port0 - CLKREQ change to Port0 - Remove DEVSLEP - Reserved PDE# for Intel SCH - Reserved Wake# for Intel SCH	
2	68	SSD	1023A	Clock P/N	Fix Clock P/N issue	
3			1027A		SE00000T600 1000P 50V K X7R 0201 change to SE170102K80 1000P 25V K X7R 0201 - C153/C160/C161/CC104/CC383/CT60/CT221 SE000013500 1U 10V M X5R 0201 change to SE00000UC00 1U 6.3V M X5R 0201 - CC33/44/45/46/47/69/70/74/75/76/77/78/79/83/84/86/88/105/106/155/156 SE000013M00 22U 10V M X5R 0603 change to SE00000M000 22U 6.3V M X5R 0603 - CT42/43/50/51/57/58 SE075223K80 0.022U 25V K X7R 0402 change to SE068103K80 0.01UF 25V K X7R 0402 - CT59 SE00001H600 2.2U 10V K X5R 0201 change to SE00000V680 2.2U 10V M X5R 0402 - CT34 SB002000080 0 +/-5% 0805 change to R_SHORT - RS18/RA3/RA4/RM9 SA00000V200 6781-1P8F change to SA00000DSK00 6788-1P81U - UF3	
4			1027B		H37 change to H_2P5	
5			1029A	For DFB issue	- EMI agree remove LV3/LV4/LV5/RV340/RV342	
6			1104A	Board ID	Add EVT2@	
7	58		1116A	Board ID	Add PVT@	
8			1116A	For BOM	UT1 / UV5 change to SA000079400	
9	58		1130A	Board ID	Add MP@ (PCB Rev 1A)	
10	16		1130A	For C10 issue	CC383 must be @ CC63 change to RC4083 100K PD	
11	81-101		1130B	POWER update	Combined Power SCH (1130A PWR)	
12	38		1201A	For Placement	Remove RV366/RV367/RV98 for placement	
13	71		1209A	DFX request	Delet LT9 dor DFX request Change RT291/RT292 to R-short	
14	81-101		0114B	POWER update	Combined Power SCH (1221A PWR)	